

# Compal Confidential

## HBL51 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M

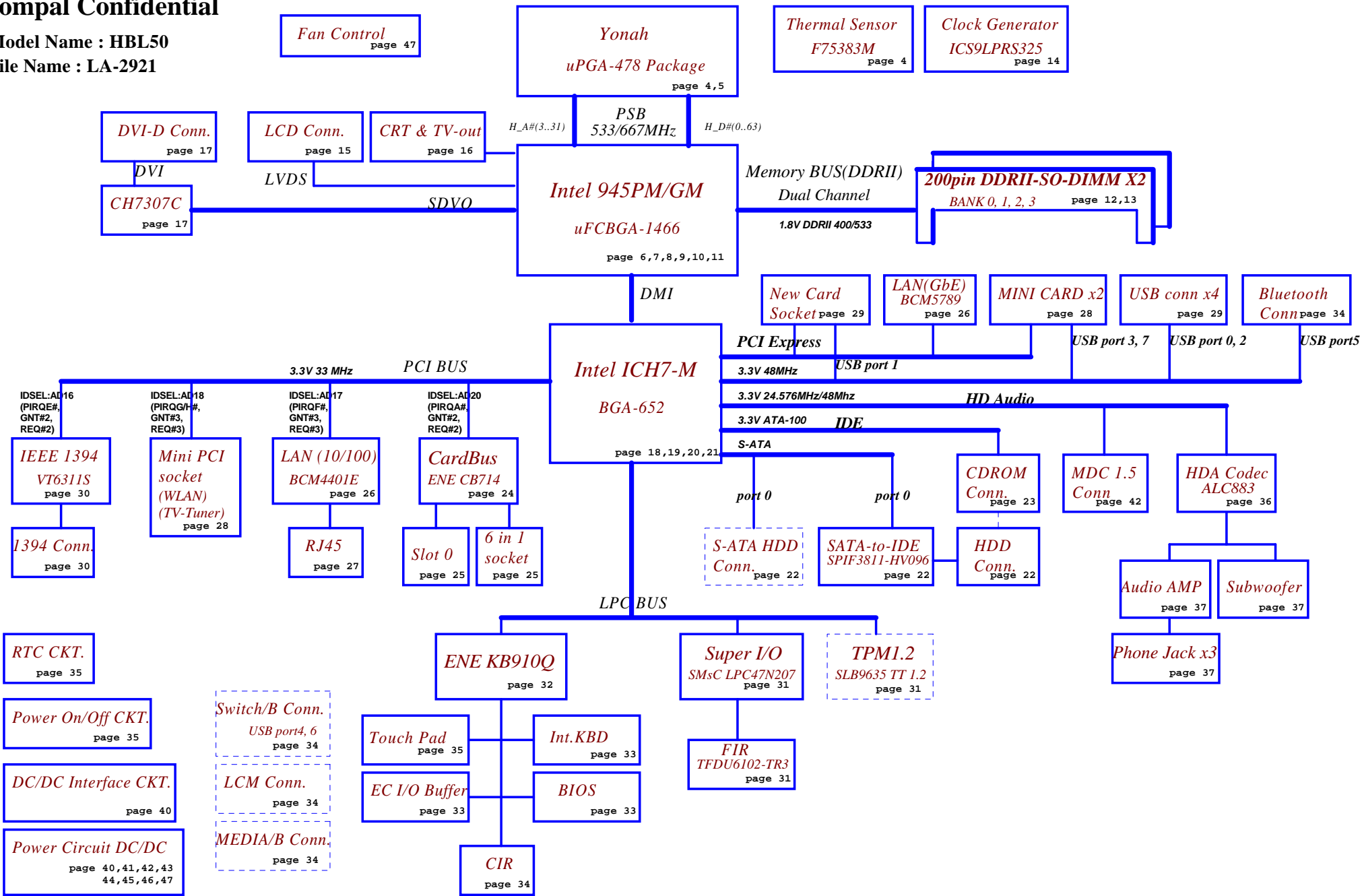
2005-11-03

REV: 0.2

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Model Name : HBL50  
File Name : LA-2921



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

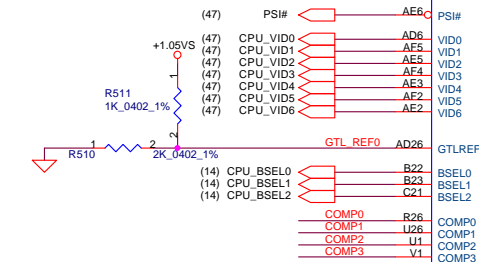
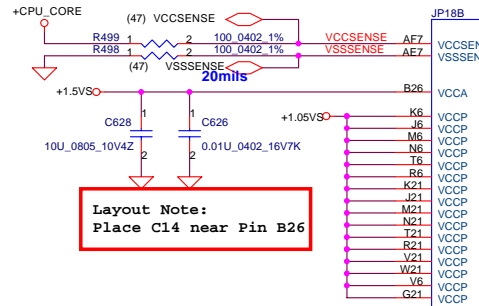
BTO Item	BOM Structure
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI_CARD1	MINI1@
MINI_CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
TVOUT	TVOUT@
1394	6311S@
CARDREADER	4IN1@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@

SKU ID Table

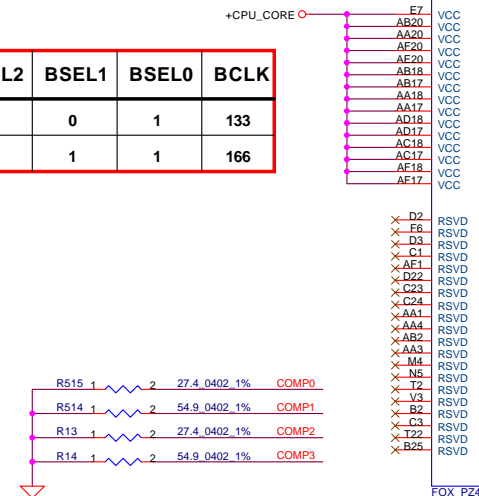
SKU ID	SKU
0	
1	GM
2	
3	
4	
5	
6	
7	



Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.40hms  
with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.



BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166

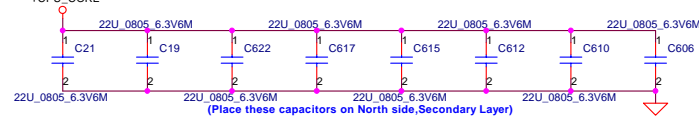
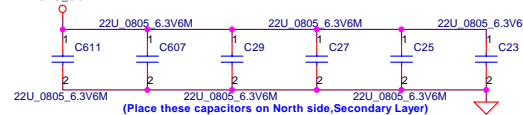
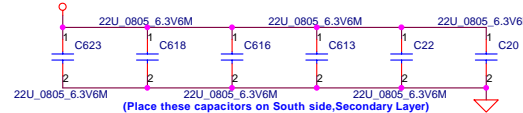
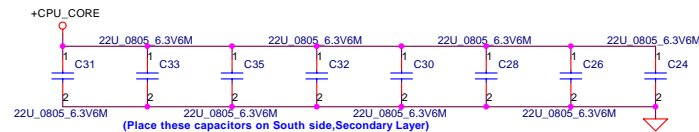
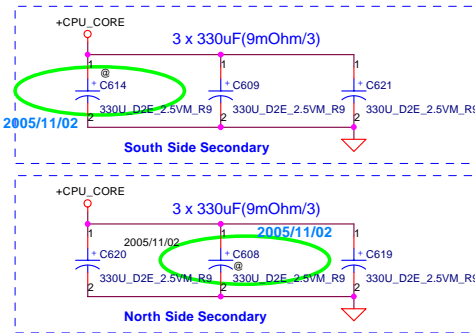
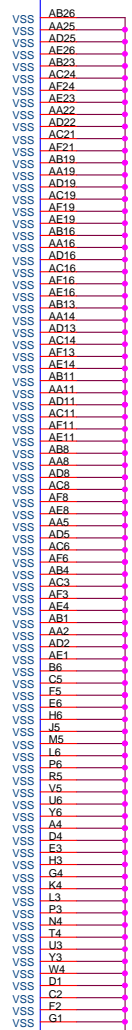


TRACE CLOSELY CPU < 0.5'

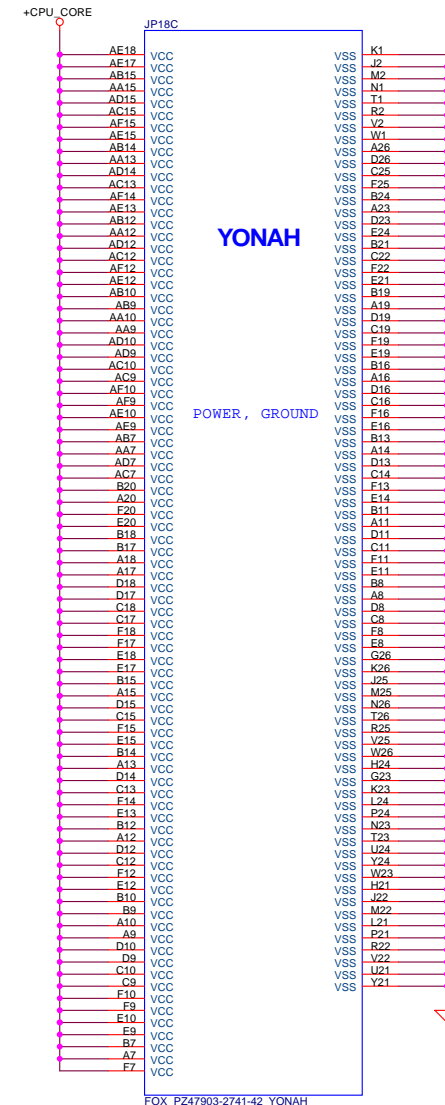
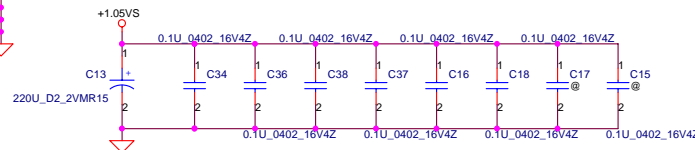
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.40hms)  
COMP1, COMP3 layout : Space 25mils (550hms)



POWER, GROUND, RESERVED SIGNALS AND NC



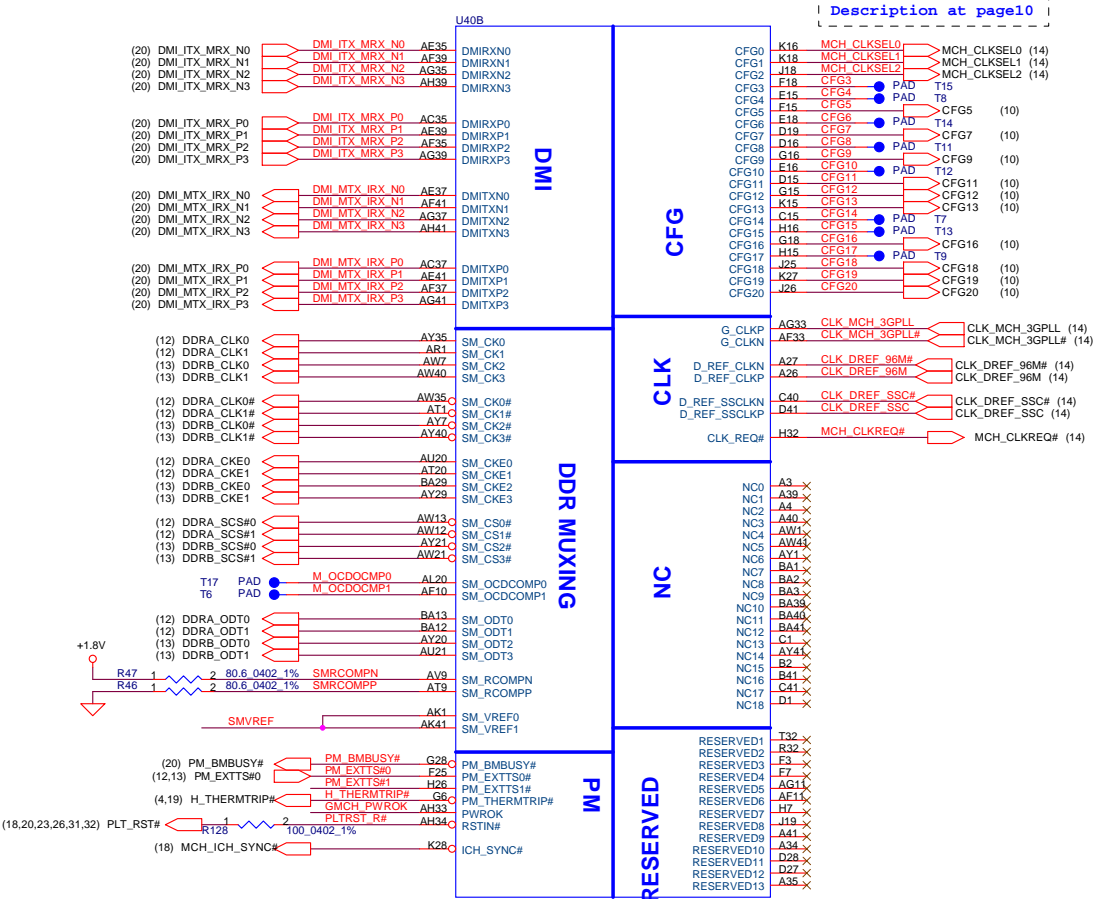
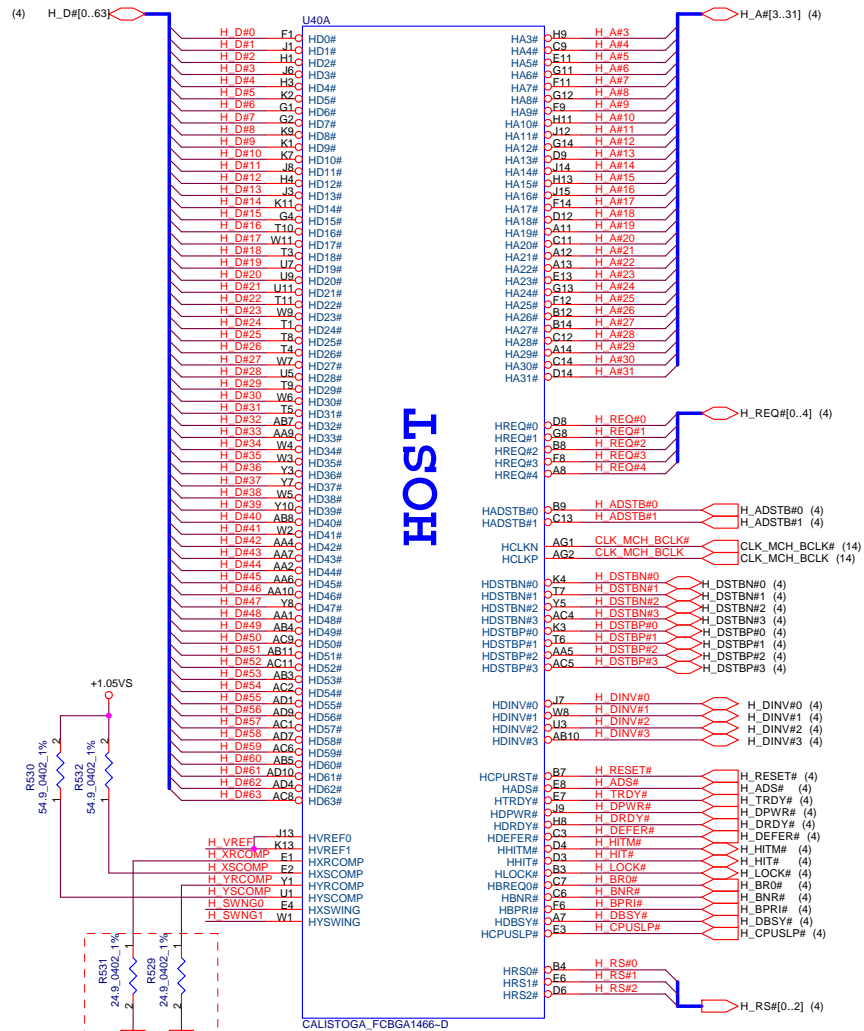
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32



## YONAH

POWER, GROUND

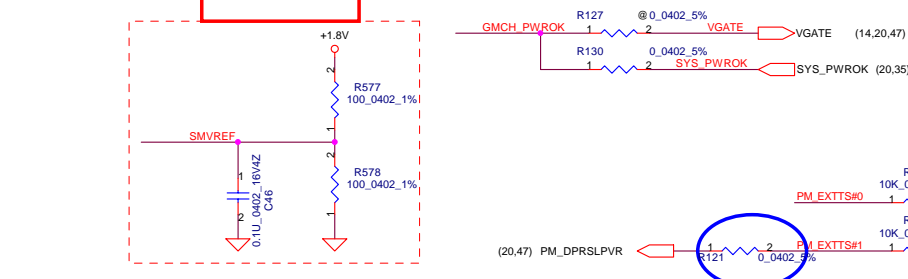
945GM(A-1)(QJ15)[ES2]: SA000005970  
945GM(A-2)(QK44)[ES3]: SA000005980  
945PM(A-2)(QK46)[ES3]: SA00000UUV10



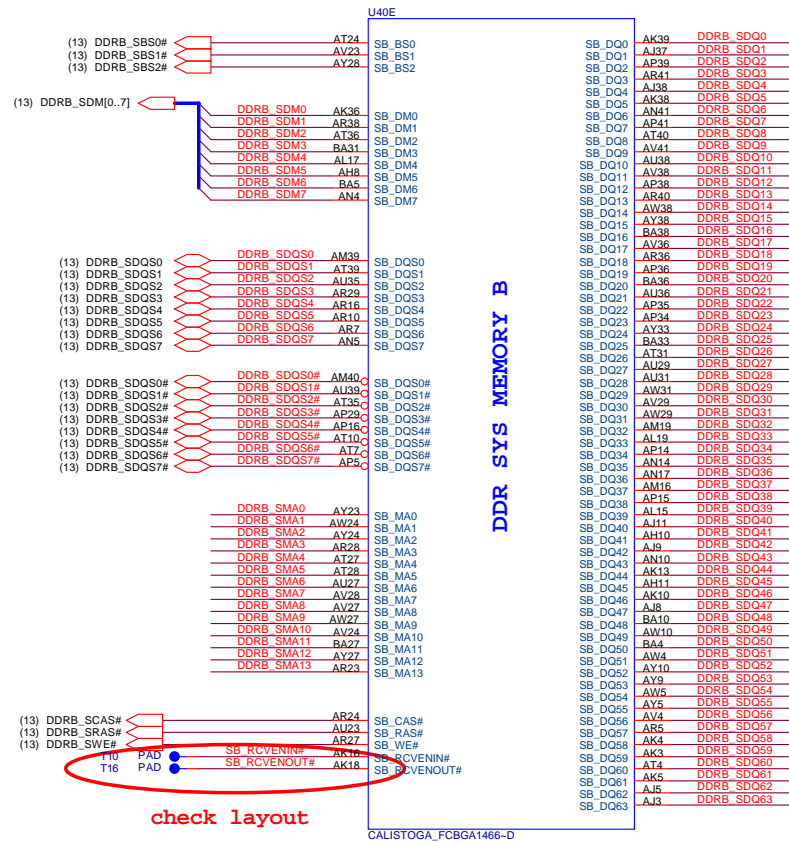
Description at page10

Layout Note:  
H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 /  
H\_SWNG1 trace width and spacing is 10/20.

Layout Note:  
SMVREF trace width and spacing is 20/20.



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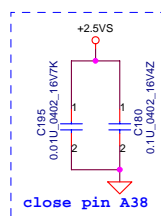
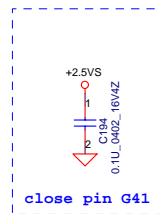
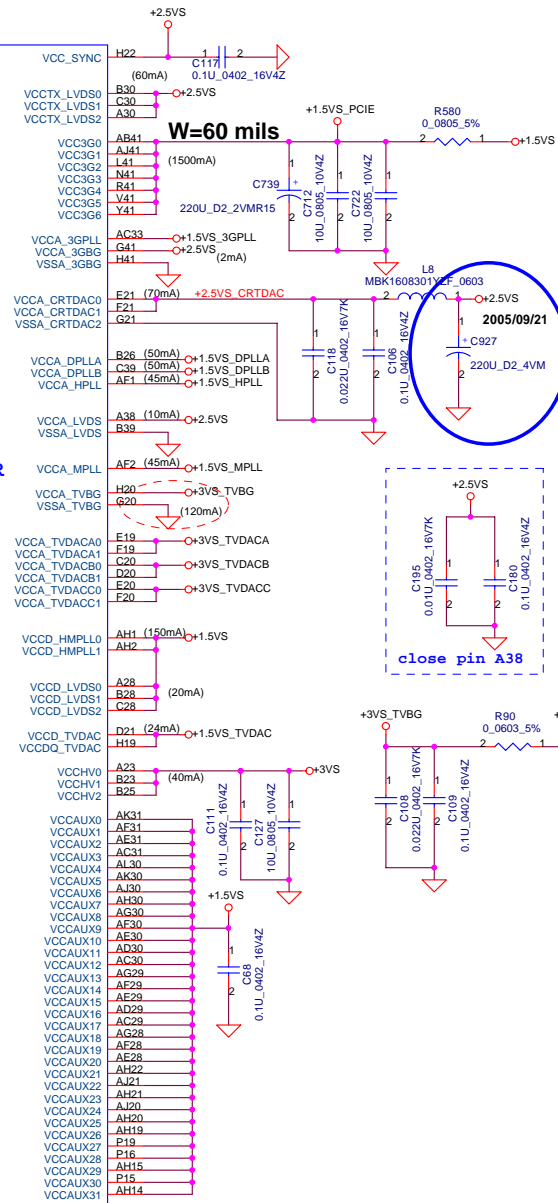




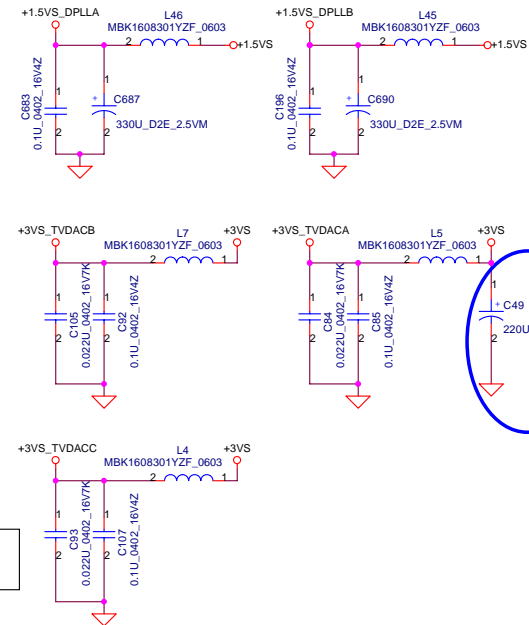


CALISTOGA\_FCBGA1466-D

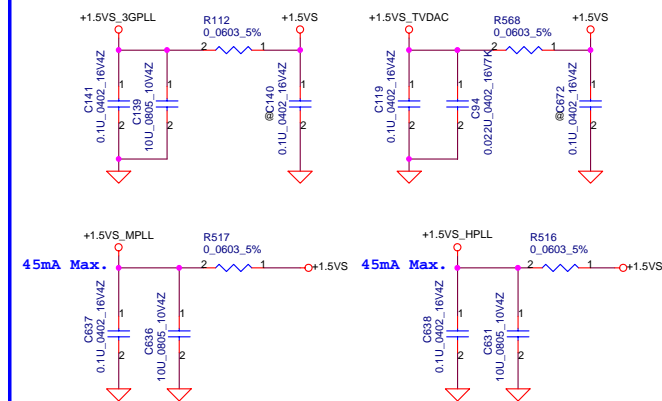
# POWER



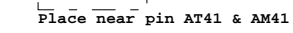
**CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Calistoga**



## PCI-E/MEM/PSB PLL decoupling



```
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down
```



(6) CFG5 R58 1 2 @ 2.2K 0402 5%

(6) CFG7 R81 1 2 @ 2.2K 0402 5%

(6) CFG9 R67 1 2 @ 2.2K 0402 5%

(6) CFG11 R57 1 2 @ 2.2K 0402 5%

(6) CFG12 R59 1 2 @ 2.2K 0402 5%

(6) CFG13 R69 1 2 @ 2.2K 0402 5%

(6) CFG16 R68 1 2 @ 2.2K 0402 5%

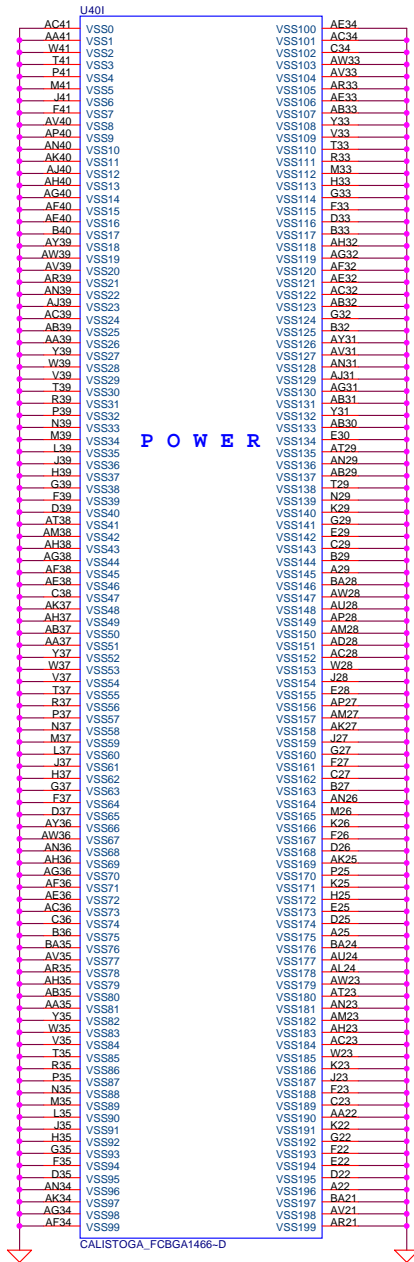
(6) CFG18 R92 1 2 @ 1K 0402 5%

(6) CFG19 R95 1 2 @ 1K 0402 5%

(6) CFG20 R118 1 2 @ 1K 0402 5%

+3VS

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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz 1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

\*\*SEL\_24M/PCICLK2=0=TESTMODE  
\*\*SEL\_PCI6/PCICLK1=0=CLKREQ5#

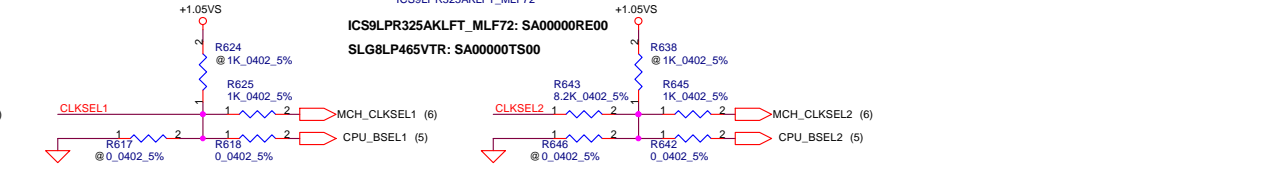
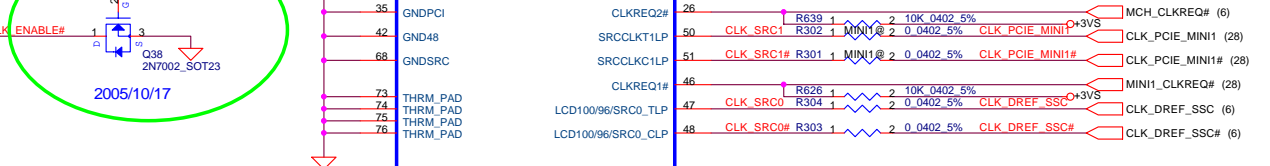
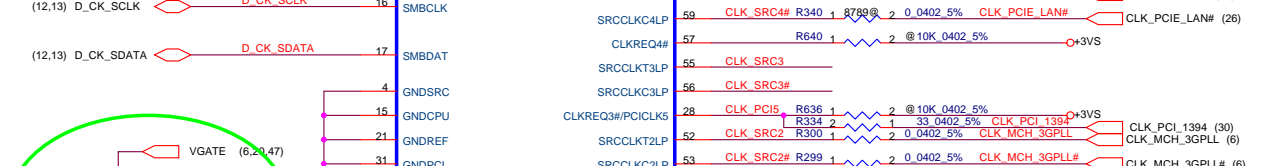
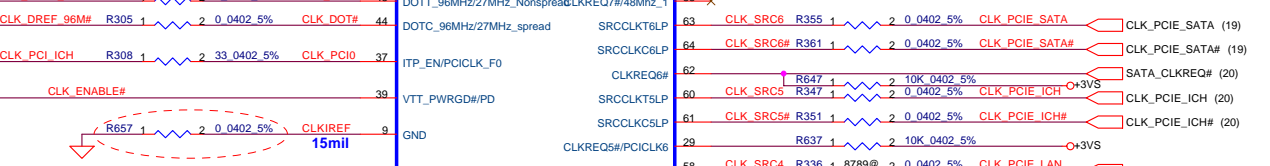
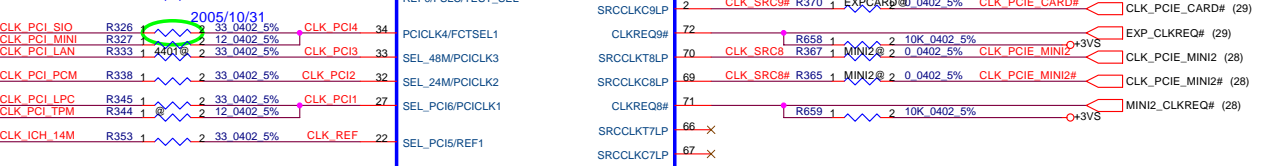
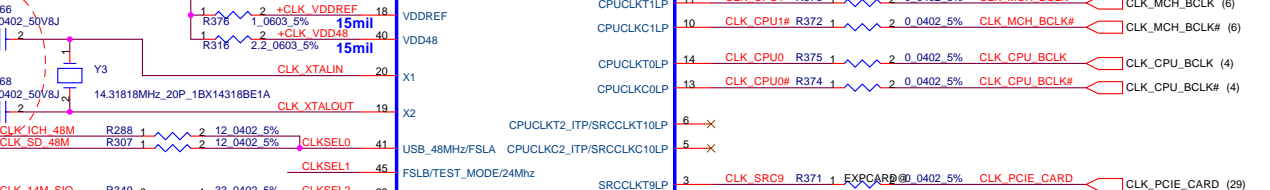
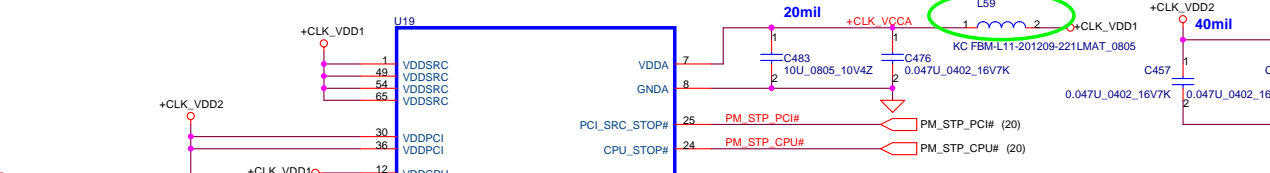
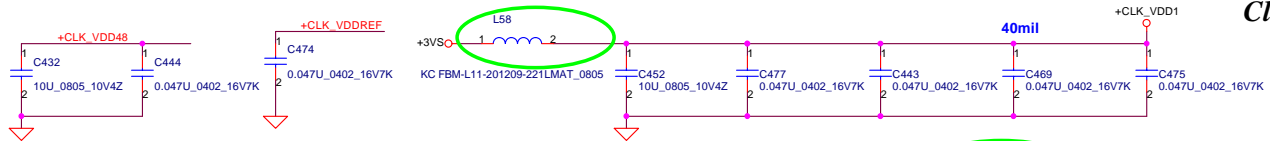
+3VS  
\*\*SEL\_PCI5=1=PCICLK5  
CLK REF  
R712 10K\_0402\_5%  
CLK PCIO  
R619 10K\_0402\_5%  
ITP\_EN/PCICLK\_F0=0=SRC pair

CLK PC14  
R713 10K\_0402\_5%  
08/29 add

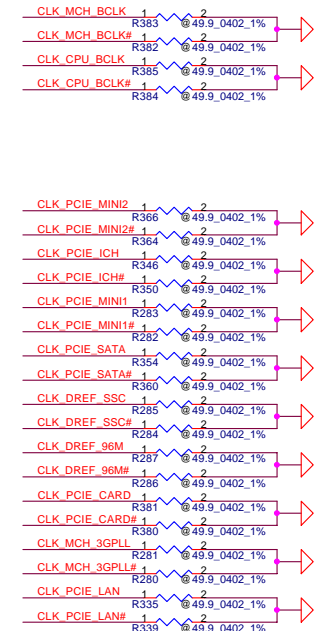
+3VS  
CLK ENABLE#  
R620 10K\_0402\_5%  
2005/10/17

+3VS  
D CK SDATA  
Q15 2N7002\_SOT23  
R387 4.7K\_0402\_5%  
+3VS  
D CK SCLK  
Q14 2N7002\_SOT23  
R386 4.7K\_0402\_5%  
+3VS

+1.05VS  
CLKSEL0  
R621 8.2K\_0402\_5%  
R622 1K\_0402\_5%  
MCH\_CLKSEL0 (6)  
R616 1K\_0402\_5%  
R615 0\_0402\_5%  
CPU\_BSEL0 (5)



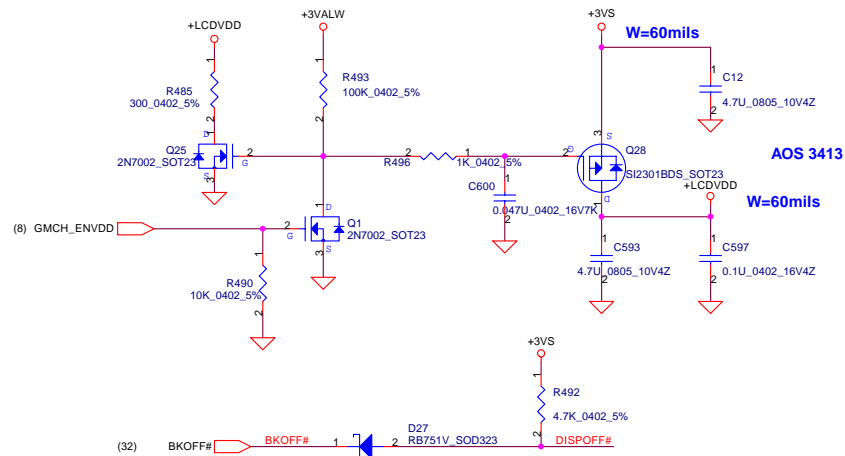
## Clock Generator



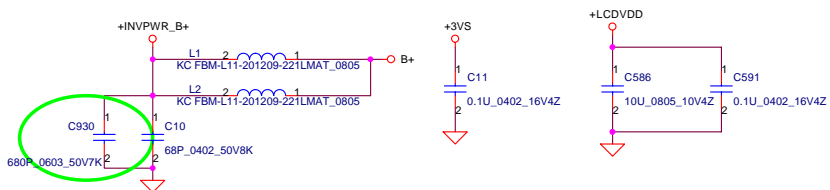
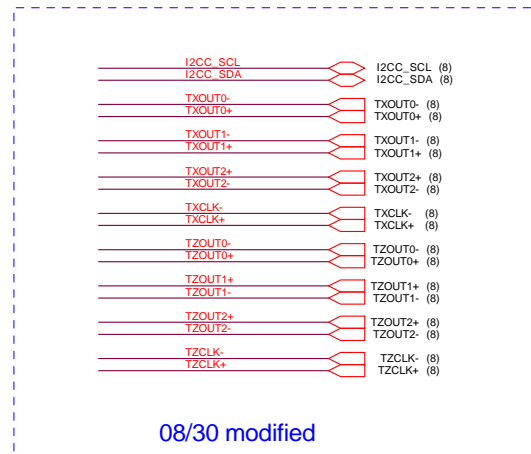
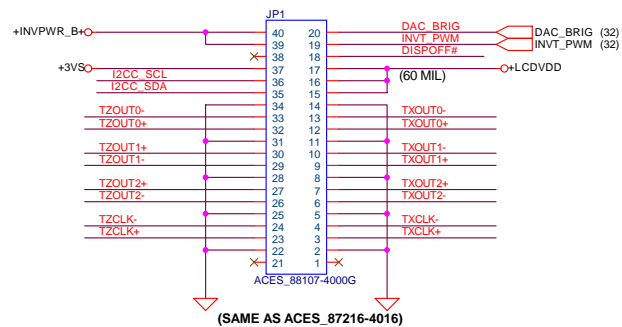
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Compal Electronics, Inc.		
Clock Generator		
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# LCD POWER CIRCUIT



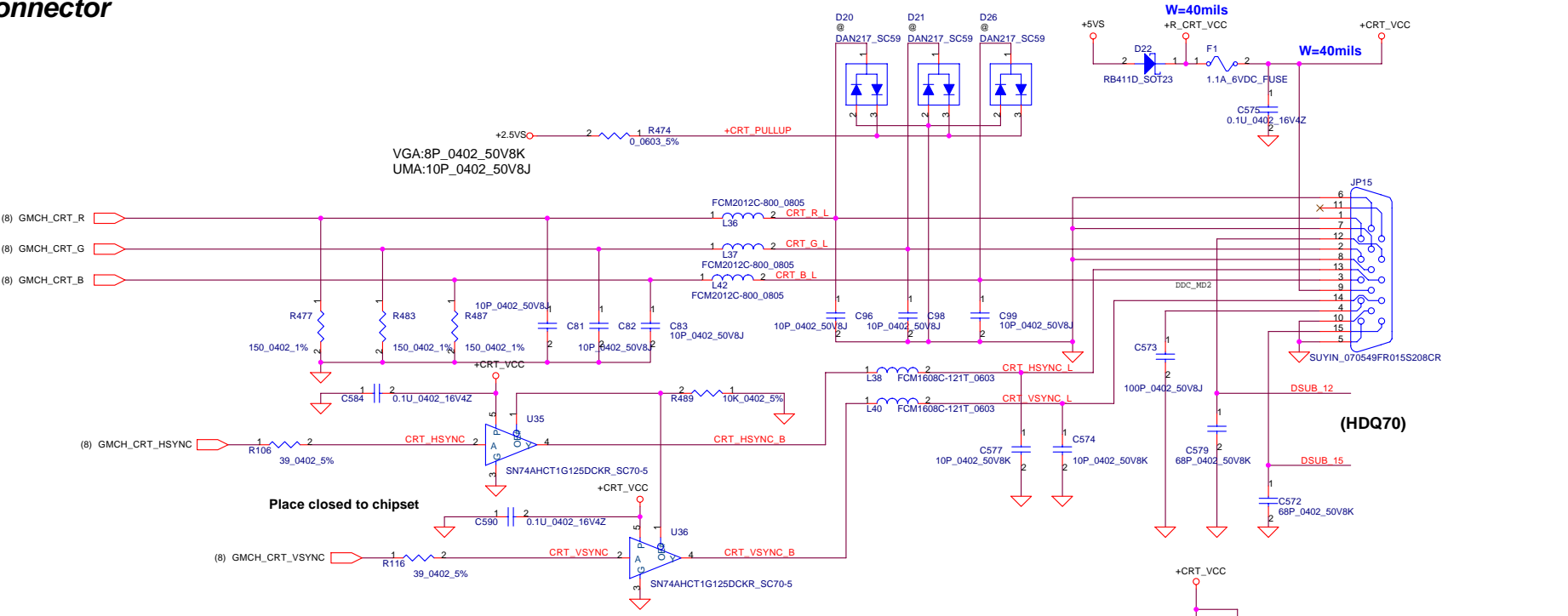
## LCD/PANEL BD. Conn.



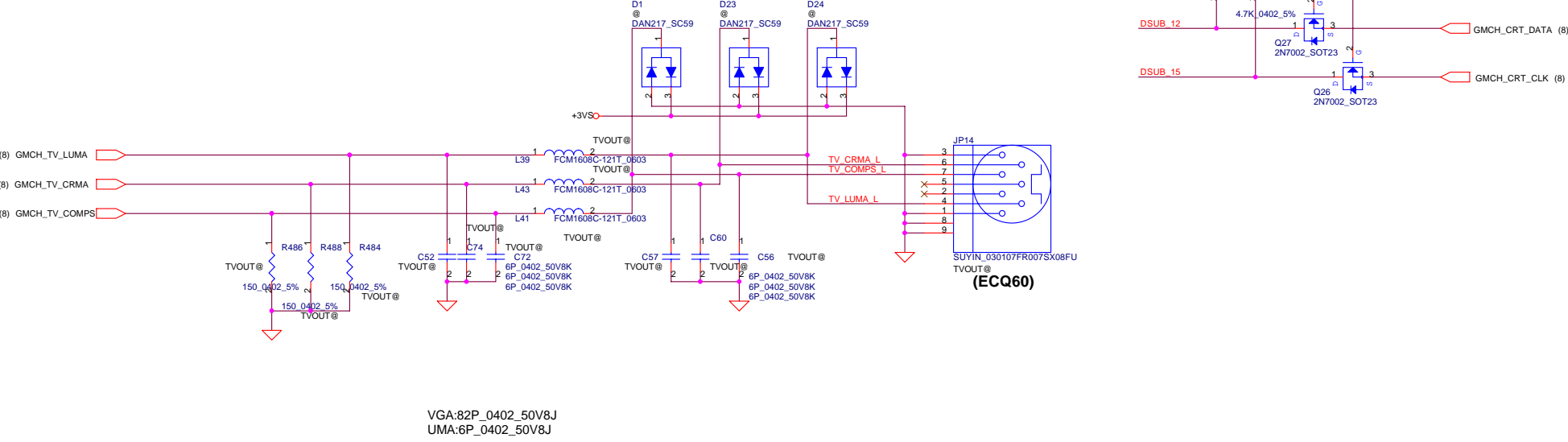
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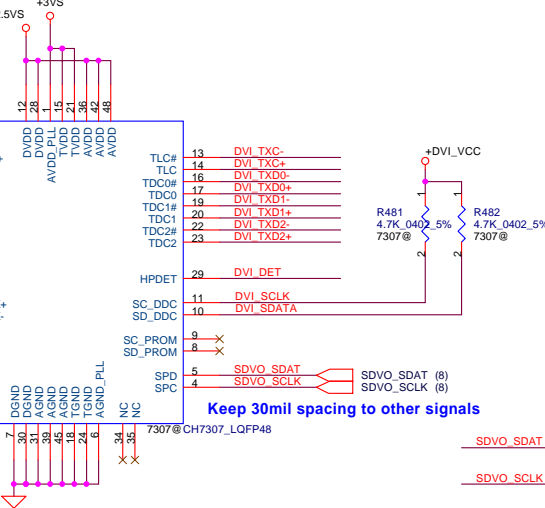
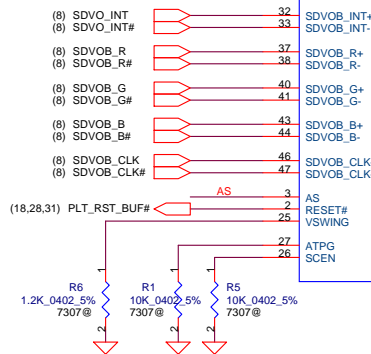
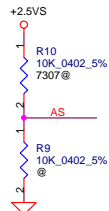
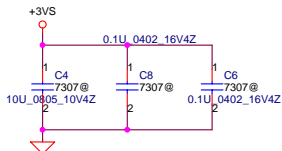
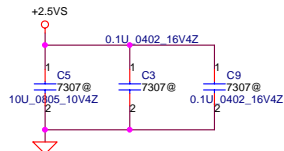
CRT Connector



TV-OUT Conn.

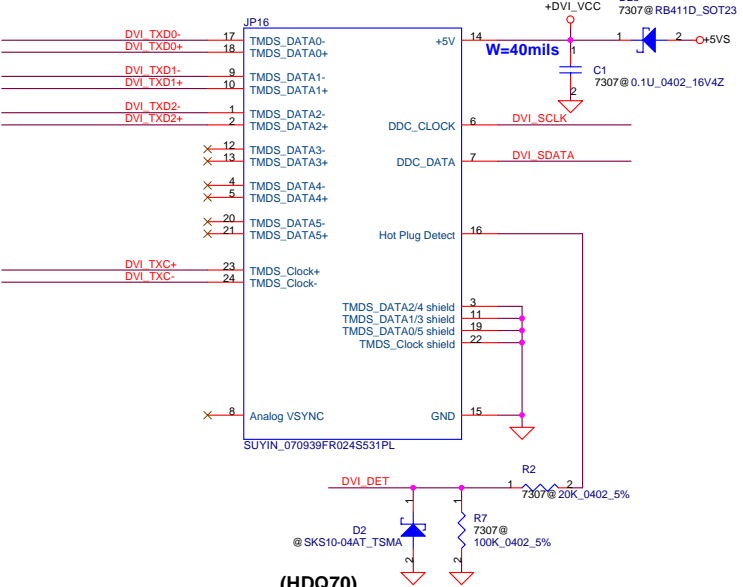


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BOM structure	DVI from SDVO
7307@	Stuff
@	No_Stuff

## DVI-D Connector

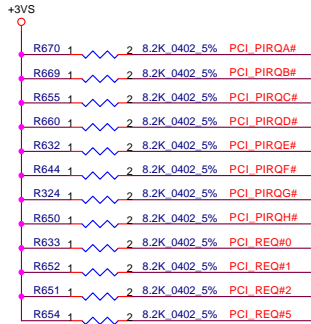
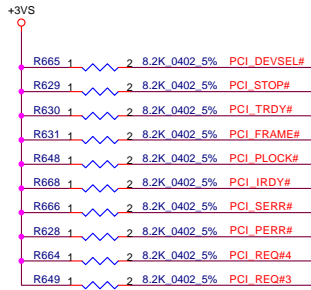


(HDQ70)

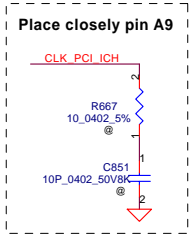
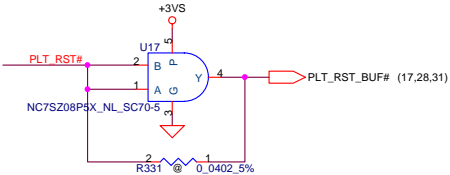
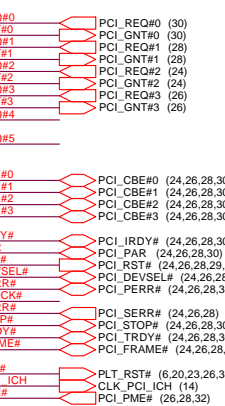
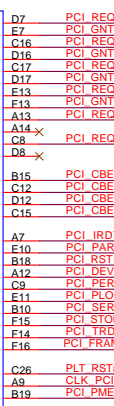
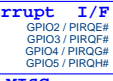
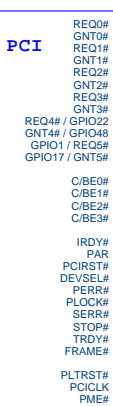
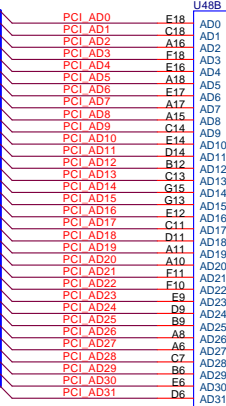
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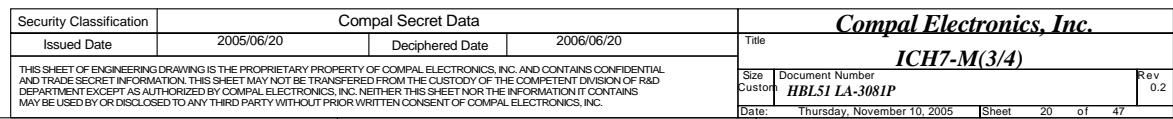
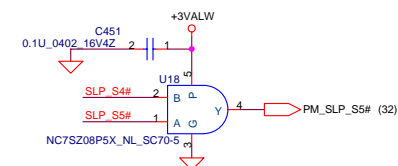
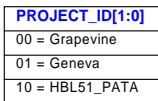


(24,26,28,30) PCI\_AD[0..31]

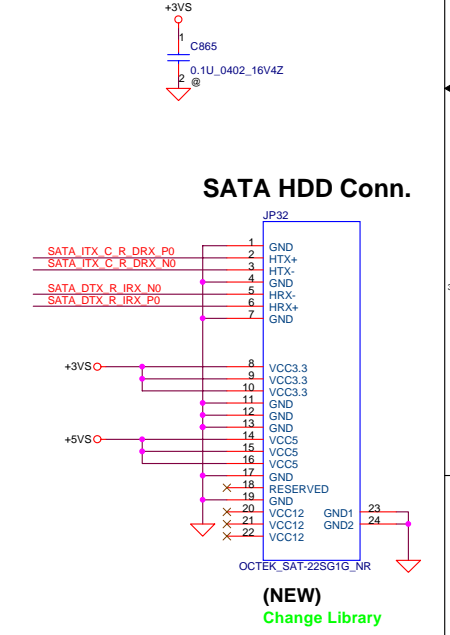
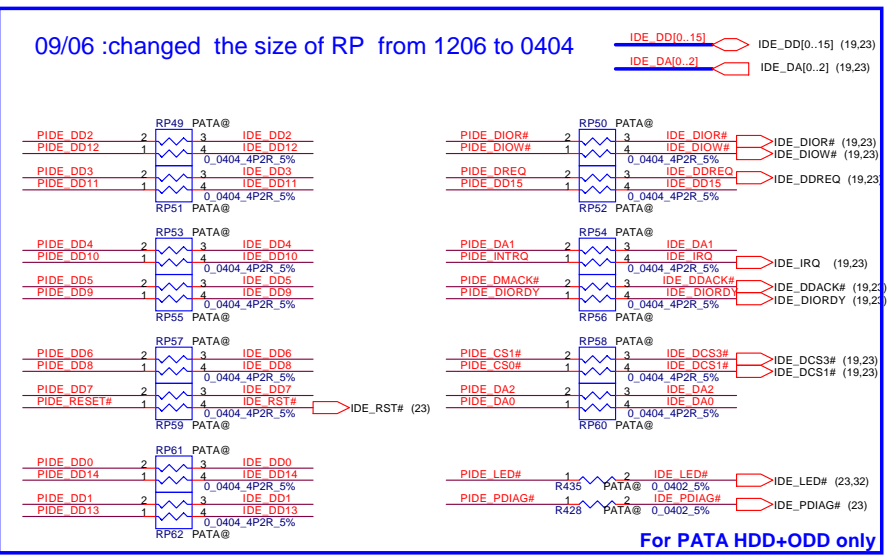
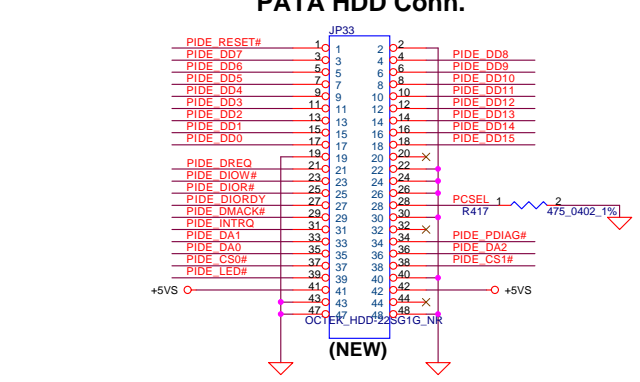
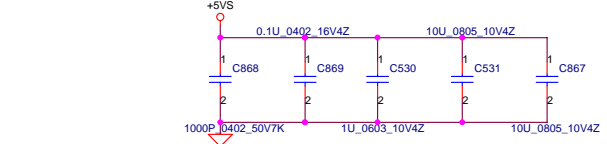
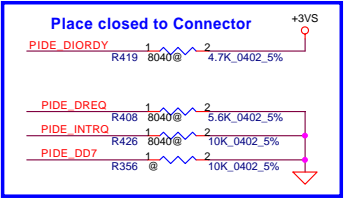
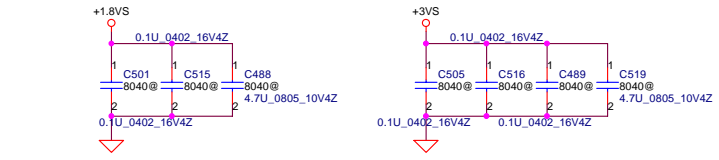
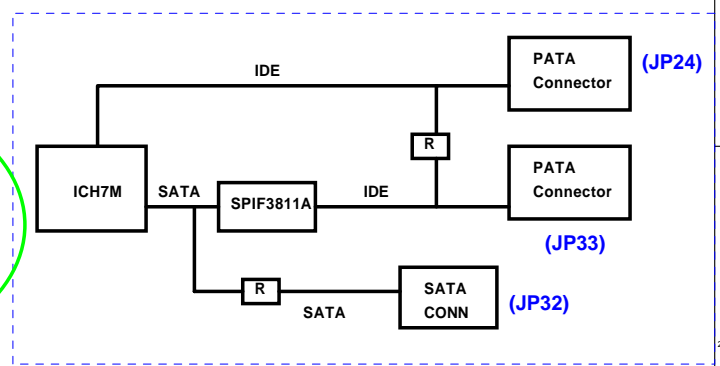
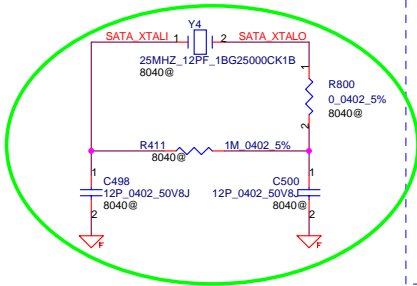
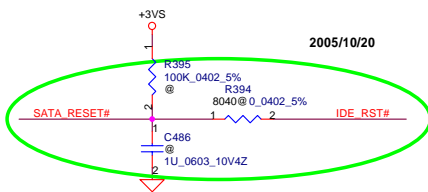
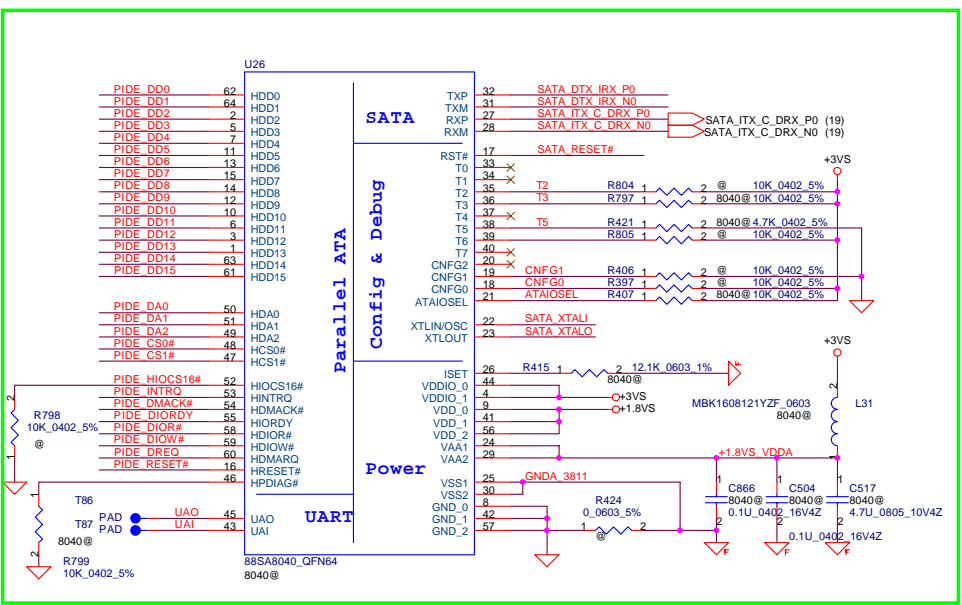


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								HBL51 LA-3081P			
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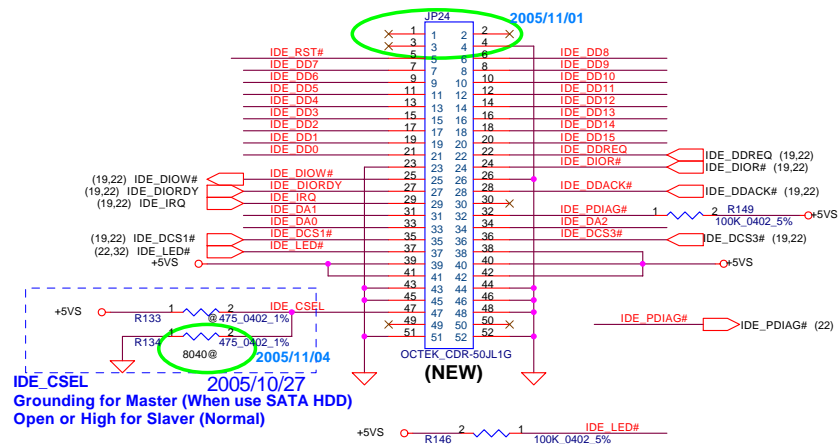
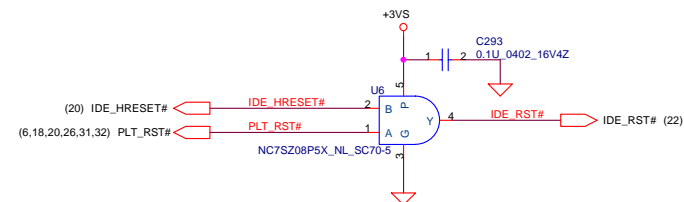
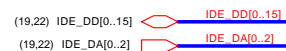
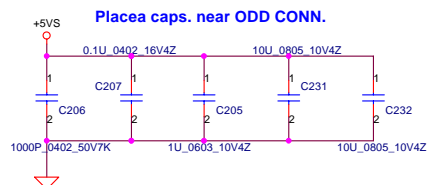




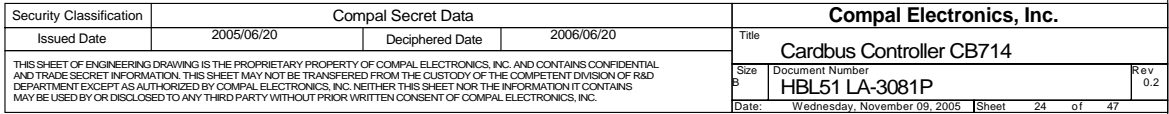


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						Size B		Document Number		Rev 0.2	
						HBL51 LA-3081P					
						Date: Wednesday, November 09, 2005				Sheet 22 of 47	
C		D		E							

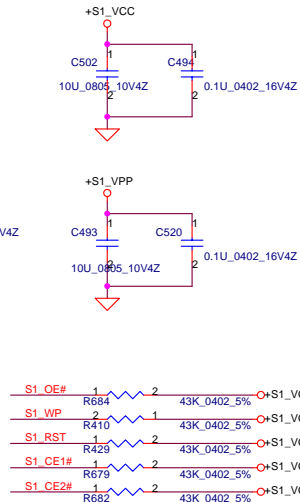
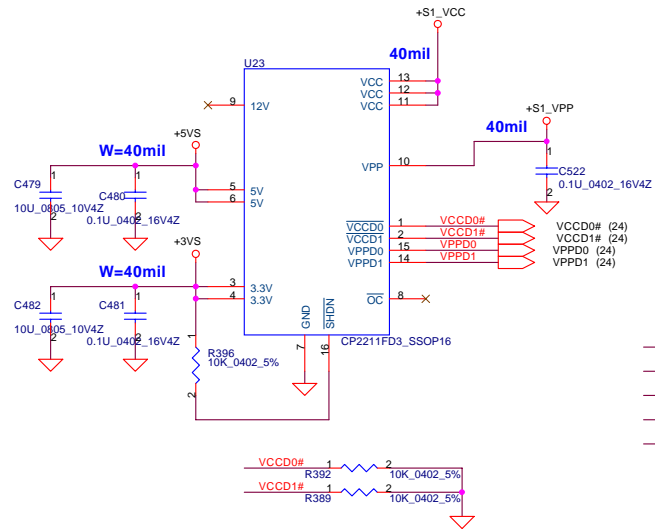




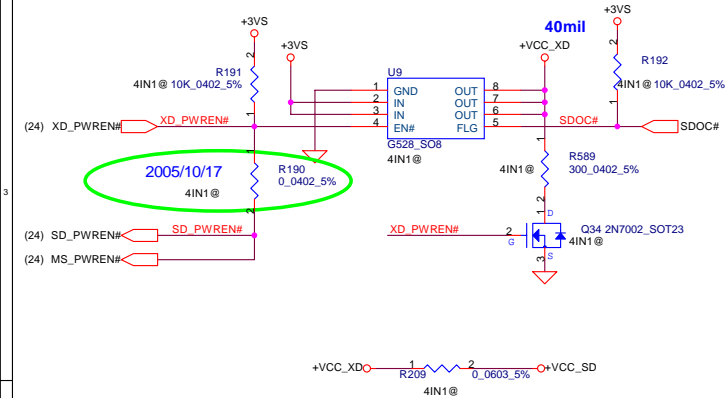
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				B	HBL51 LA-3081P
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Date: Wednesday, November 09, 2005				Sheet 23	of 47



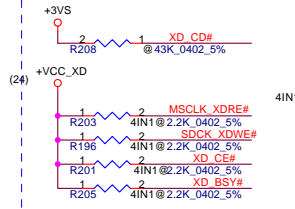
## PCMCIA Power Control



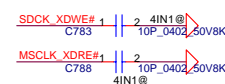
***SD/MS Power Control***  
***XD Power Control***



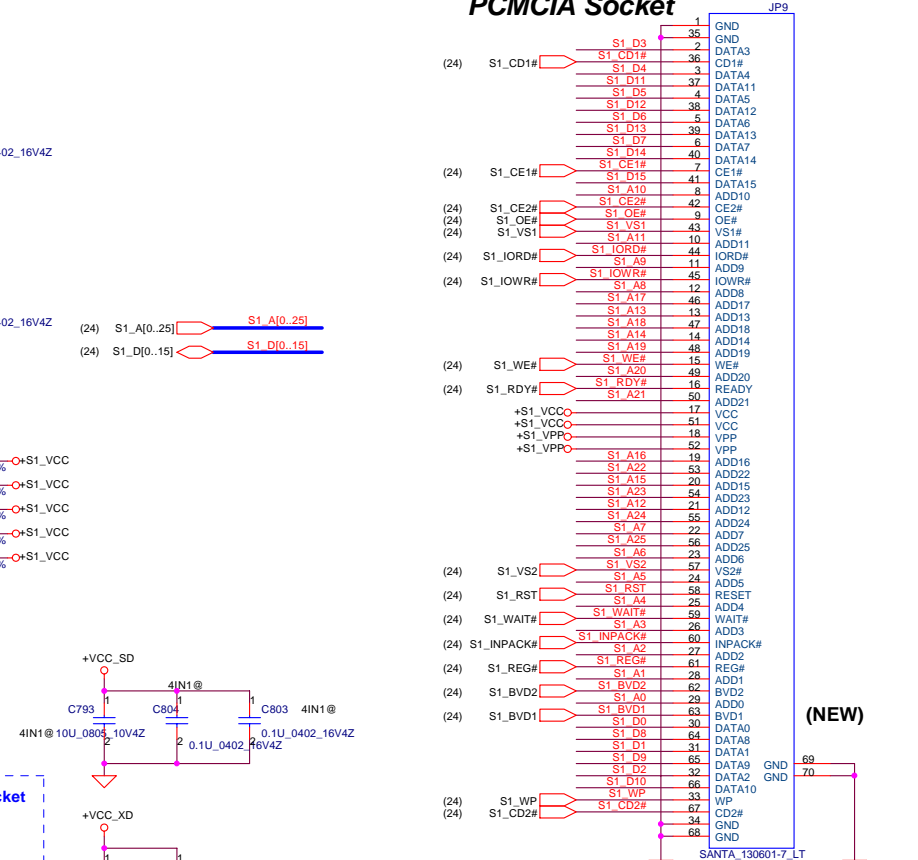
**xD PU and PD. Close to Socket**



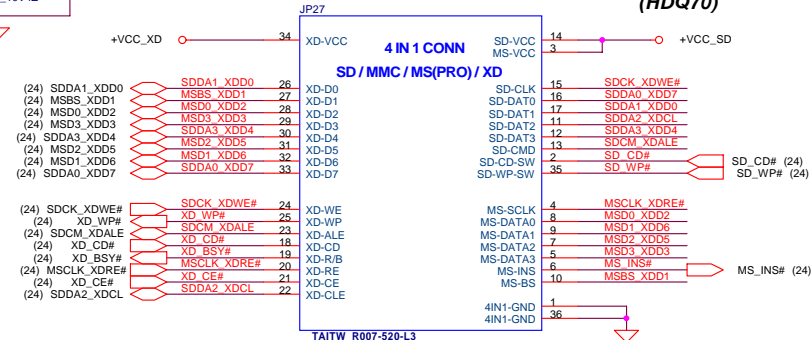
Reserve for SD,MS CLK.  
Close to Socket



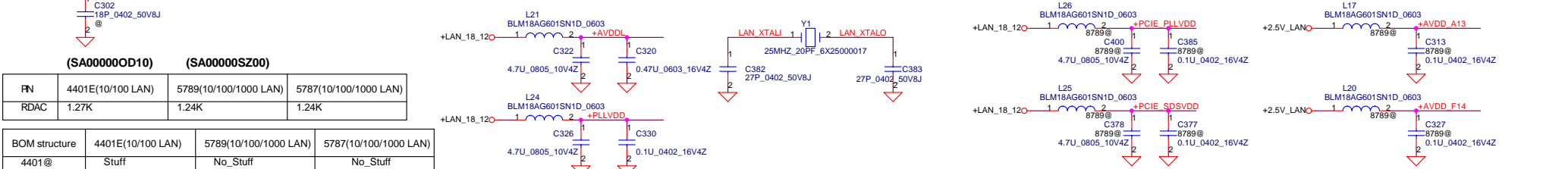
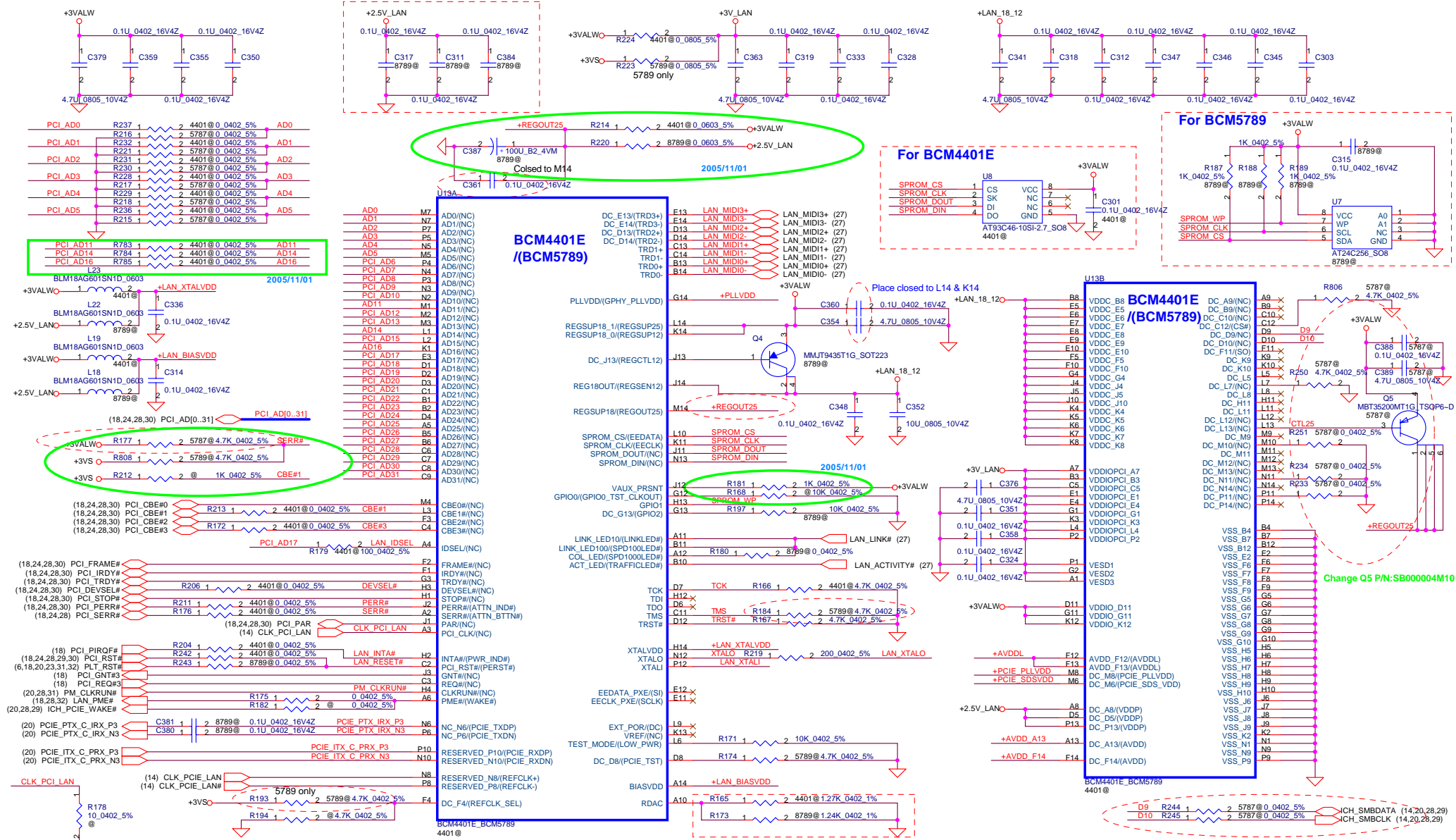
### PCMCIA Socket



**4 IN 1 Socket**  
(HDQ70)



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(SA000000D10)		(SA000000SZ00)	
PN	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
RDAC	1.27K	1.24K	1.24K

BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

Security Classification		Compal Secret Data	
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Title			
LAN BCM4401E/Jade15			
Size	Document Number	Rev	
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## LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)

# LAN BCM4401E/ BCM5789

**Place these components colsed to LAN chip  
unpop when use BCM4401E(10/100)**

The schematic illustrates the LAN interface circuitry for the BCM4401E/BCM5789 chips. It includes several key sections:

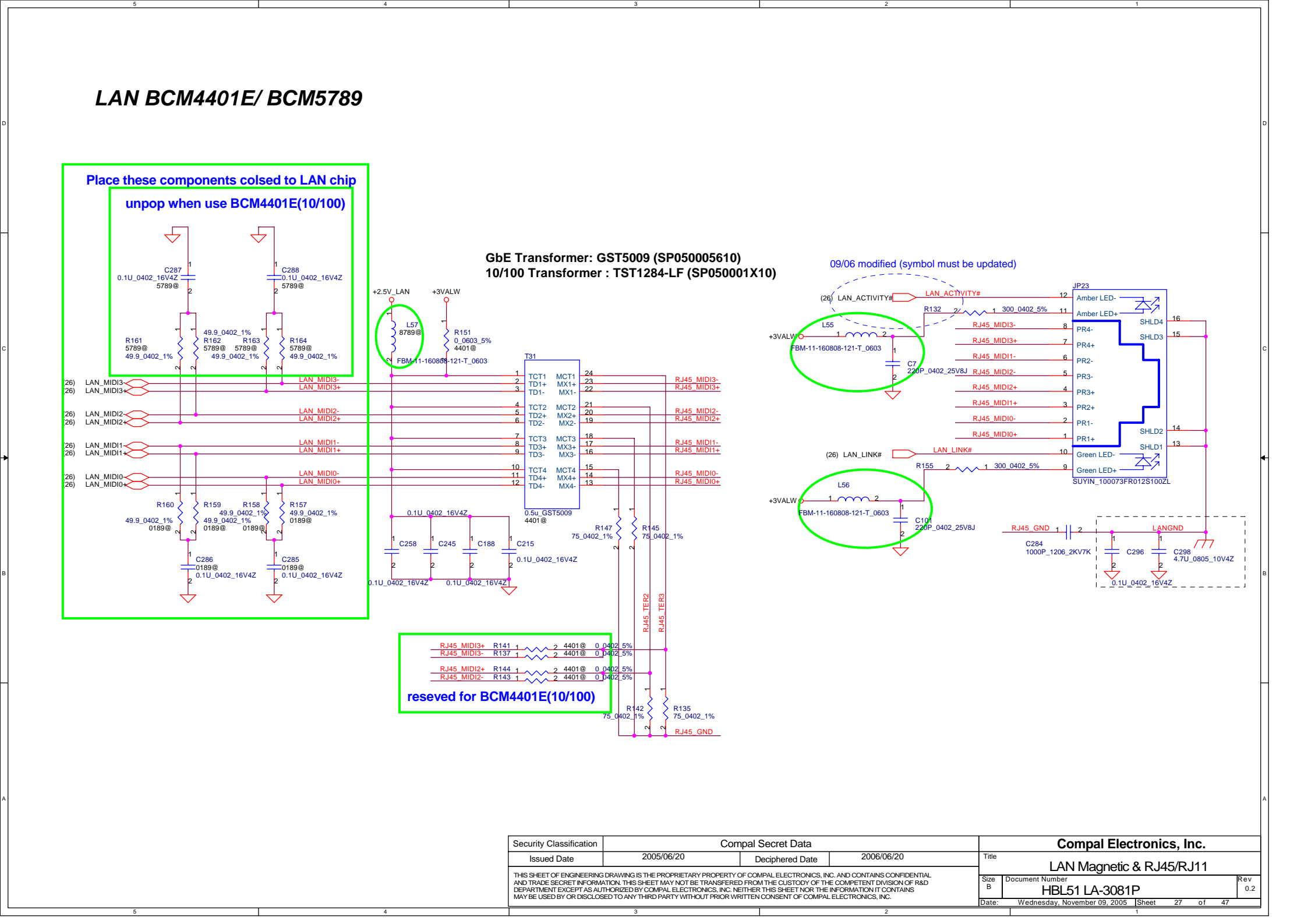
- Component Placement (Green Box):** A callout box specifies that certain components (C287, C288, R161, R162, R163, R164) should be placed close to the LAN chip and are not populated when using the BCM4401E(10/100).
- Transformer Selection:** The diagram provides guidance on selecting between a GbE Transformer (GST5009, SP050005610) and a 10/100 Transformer (TST1284-LF, SP050001X10) based on the required network speed.
- RJ45 and RJ11 Connections:** Detailed wiring is shown for RJ45 ports (MIDI3+, MIDI3-, MIDI2+, MIDI2-, MIDI1+, MIDI1-, MIDI0+, MIDI0-) and RJ11 ports (TER2, TER3). Components like resistors (R141-R143), capacitors (C245-C247), and transformers (L55, L56) are specified.
- LED Indicators:** The circuit includes connections for Amber LED+/- and Green LED+/- through the JP23 connector, utilizing components like SHLD4, SHLD3, SHLD2, and SHLD1.
- Power and Grounding:** Power supply rails (+2.5V\_LAN, +3VALW) and ground connections (RJ45\_GND, LANGND) are clearly defined throughout the schematic.

**GbE Transformer: GST5009 (SP050005610)  
10/100 Transformer : TST1284-LF (SP050001X10)**

**09/06 modified (symbol must be updated)**

**revised for BCM4401E(10/100)**

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# LAN BCM4401E/ BCM5789

**Place these components colsed to LAN chip  
unpop when use BCM4401E(10/100)**

The schematic shows the LAN interface circuitry. Key components include:

- Transformer Selection:** GbE Transformer: GST5009 (SP050005610), 10/100 Transformer : TST1284-LF (SP050001X10).
- Component Placement:** A green box highlights components to be placed close to the LAN chip, which are unpopulated when using BCM4401E(10/100). These include capacitors C287, C288, resistors R161, R162, R163, R164, and others.
- Power and Grounding:** Power rails +2.5V\_LAN and +3VALW are shown. Grounding points for RJ45\_GND and LANGND are indicated.
- RJ45 and RJ11 Connections:** The diagram shows the wiring for RJ45\_MIDI3+, RJ45\_MIDI3-, RJ45\_MIDI2+, RJ45\_MIDI2-, RJ45\_MIDI1+, RJ45\_MIDI1-, RJ45\_MIDI0+, and RJ45\_MIDI0-. It also includes RJ45\_TER2 and RJ45\_TER3 terminals.
- LED Indicators:** Amber LED+ and Green LED+ are connected to the LAN\_ACTIVITY# and LAN\_LINK# signals respectively.

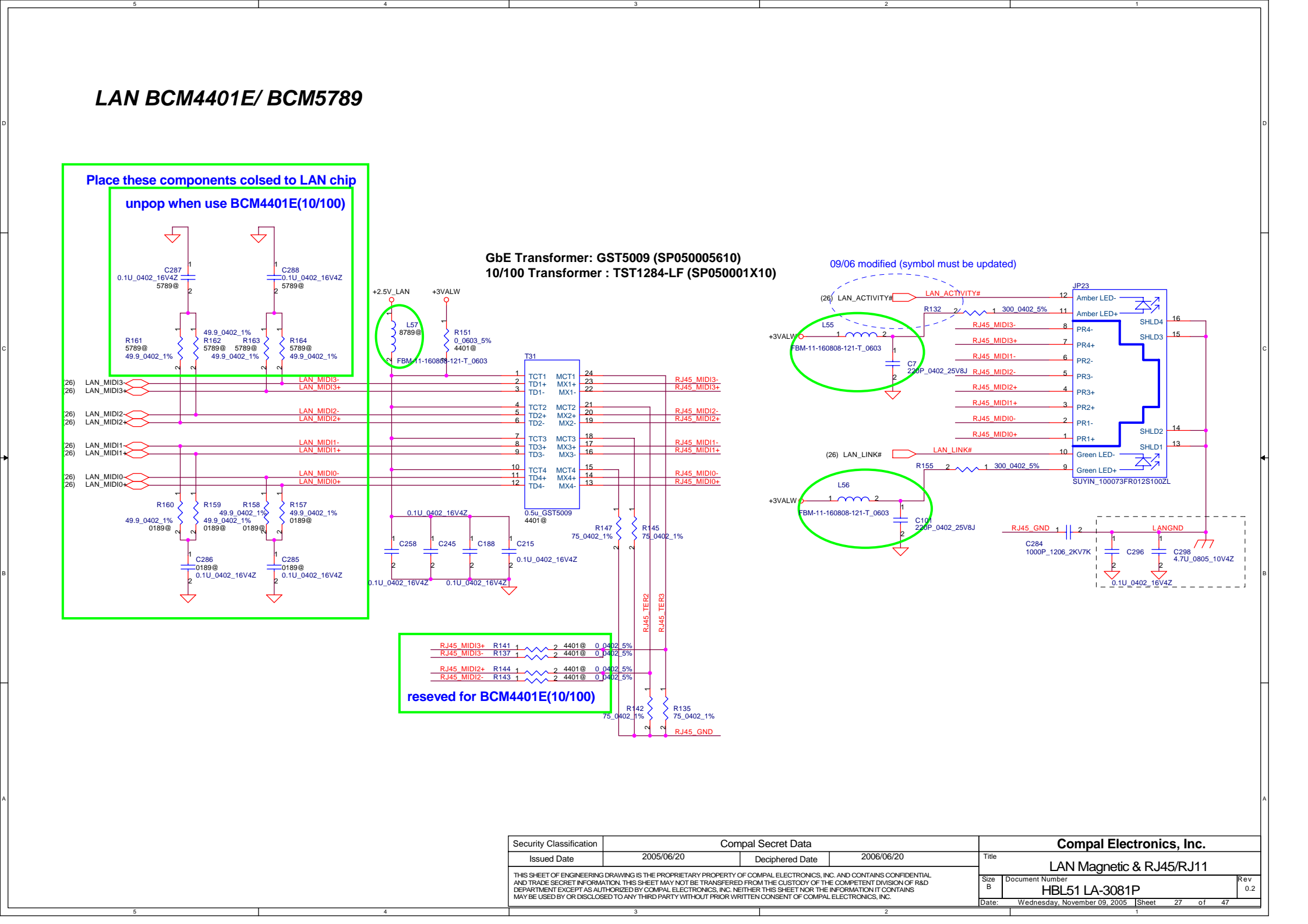
**reseeded for BCM4401E(10/100)**

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## LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

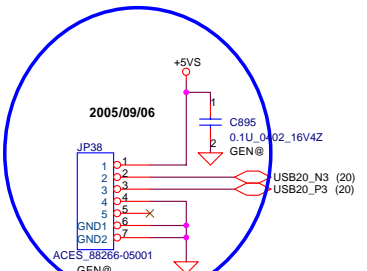
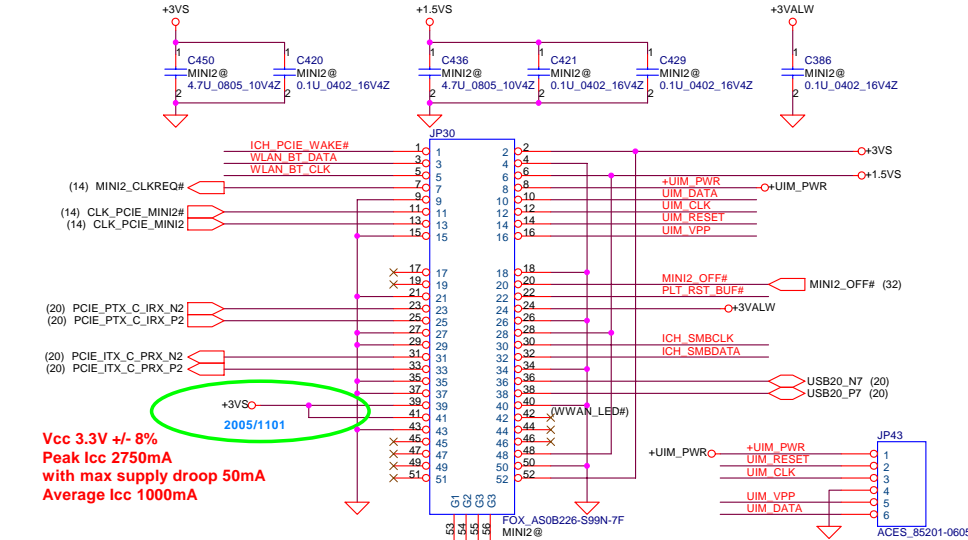
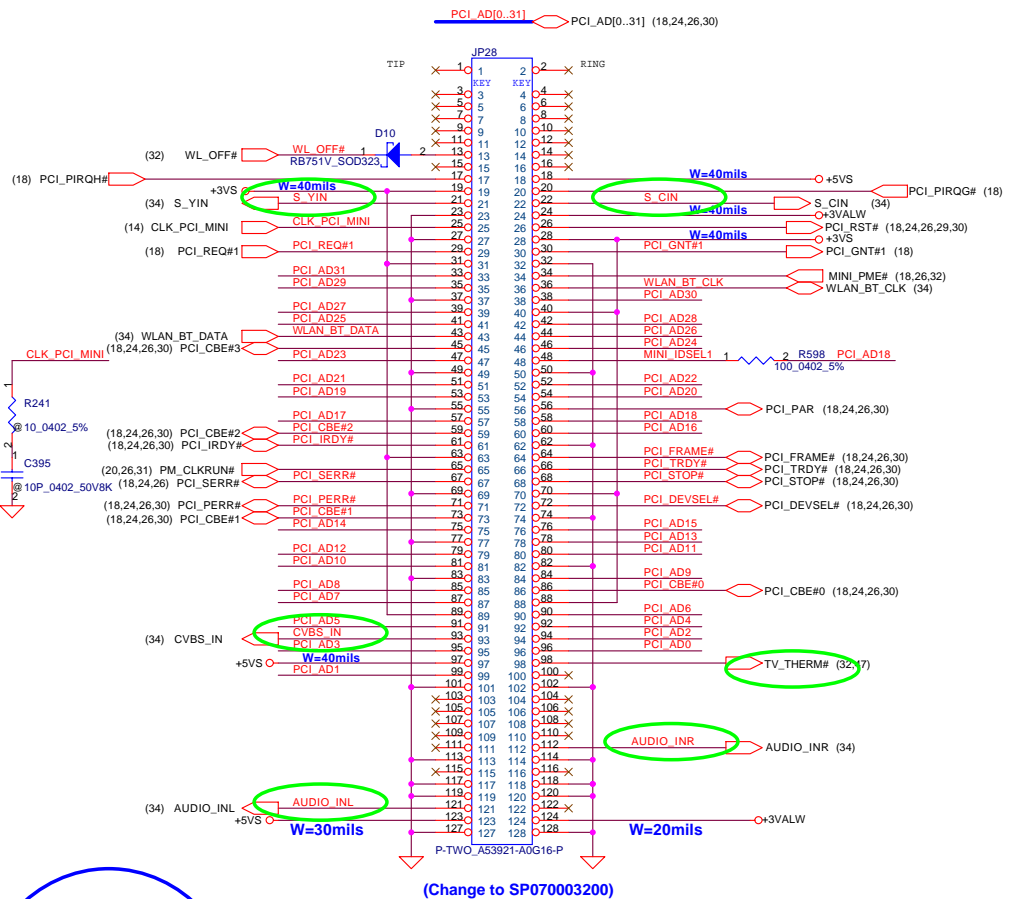
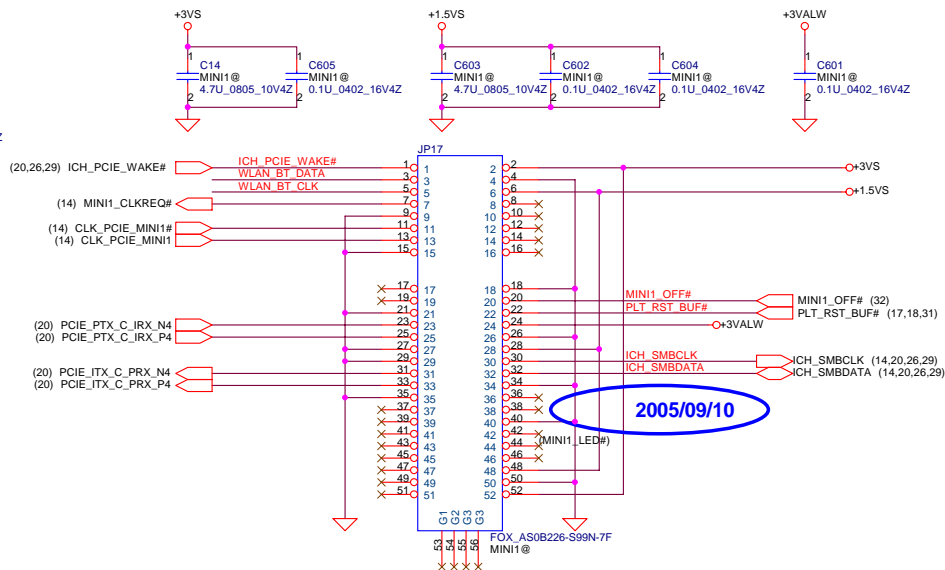
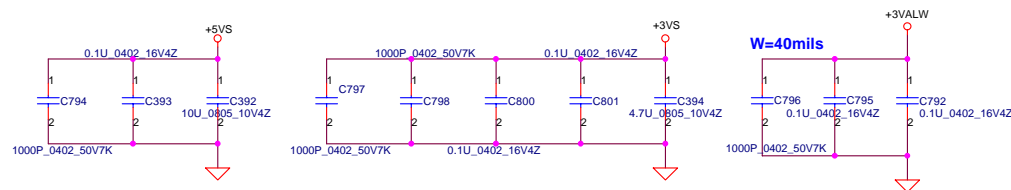
unpop when use BCM4401E(10/100)



## LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

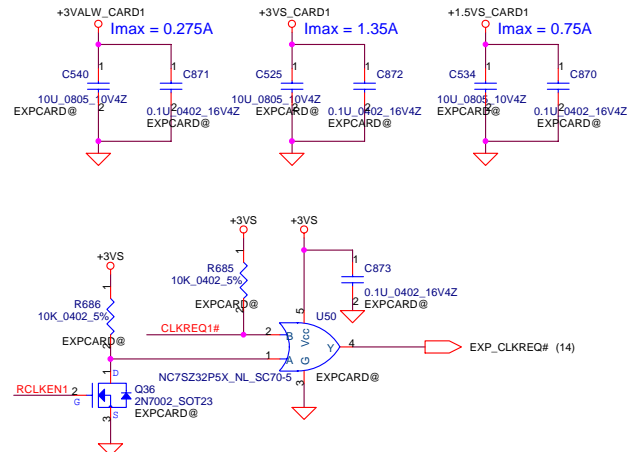
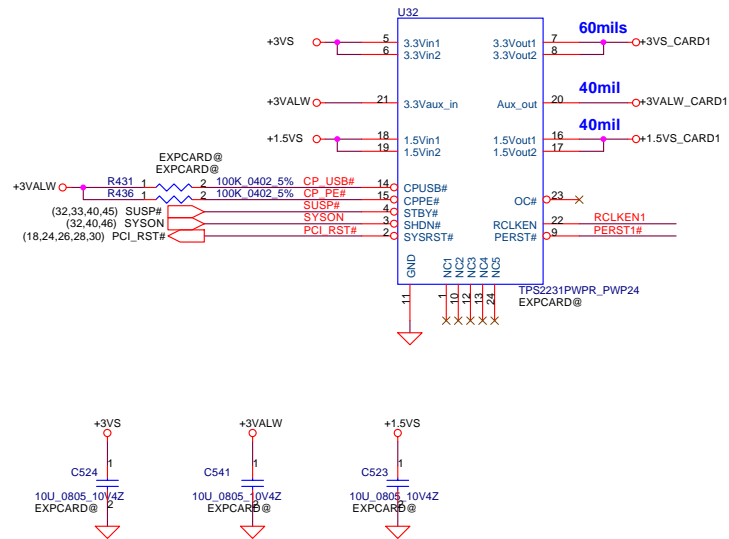
unpop when use BCM4401E(10/100)



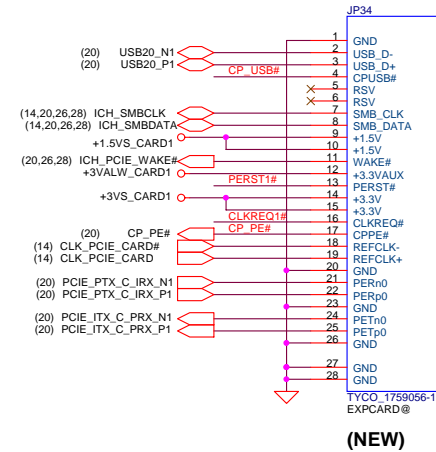
Mini Card Power Rating			
Power	Primary Power (mA)	Auxiliary Power (mA)	
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



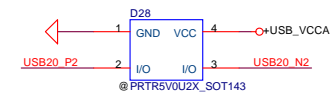
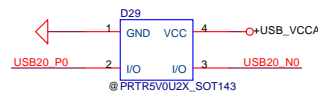
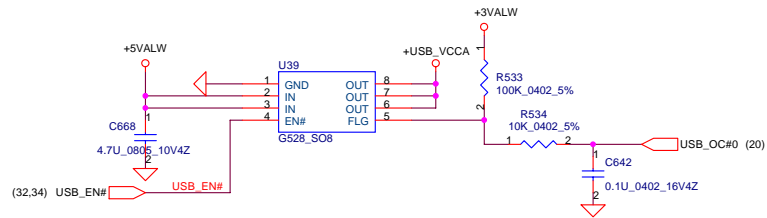
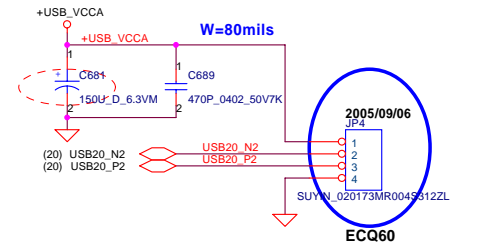
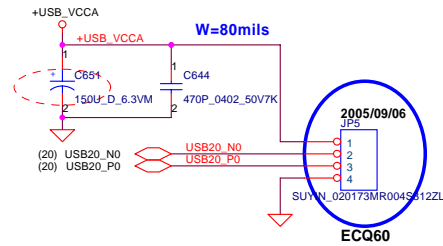
## New Card Power Switch



### ***New Card Socket (Left)***



### USB CONN. 1 & 2

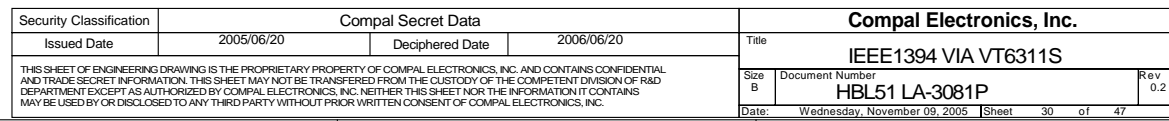
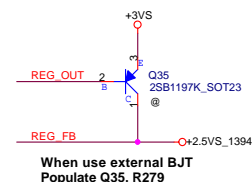
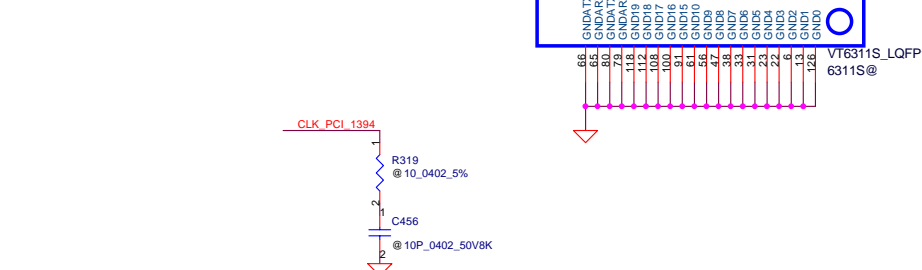
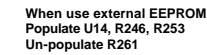


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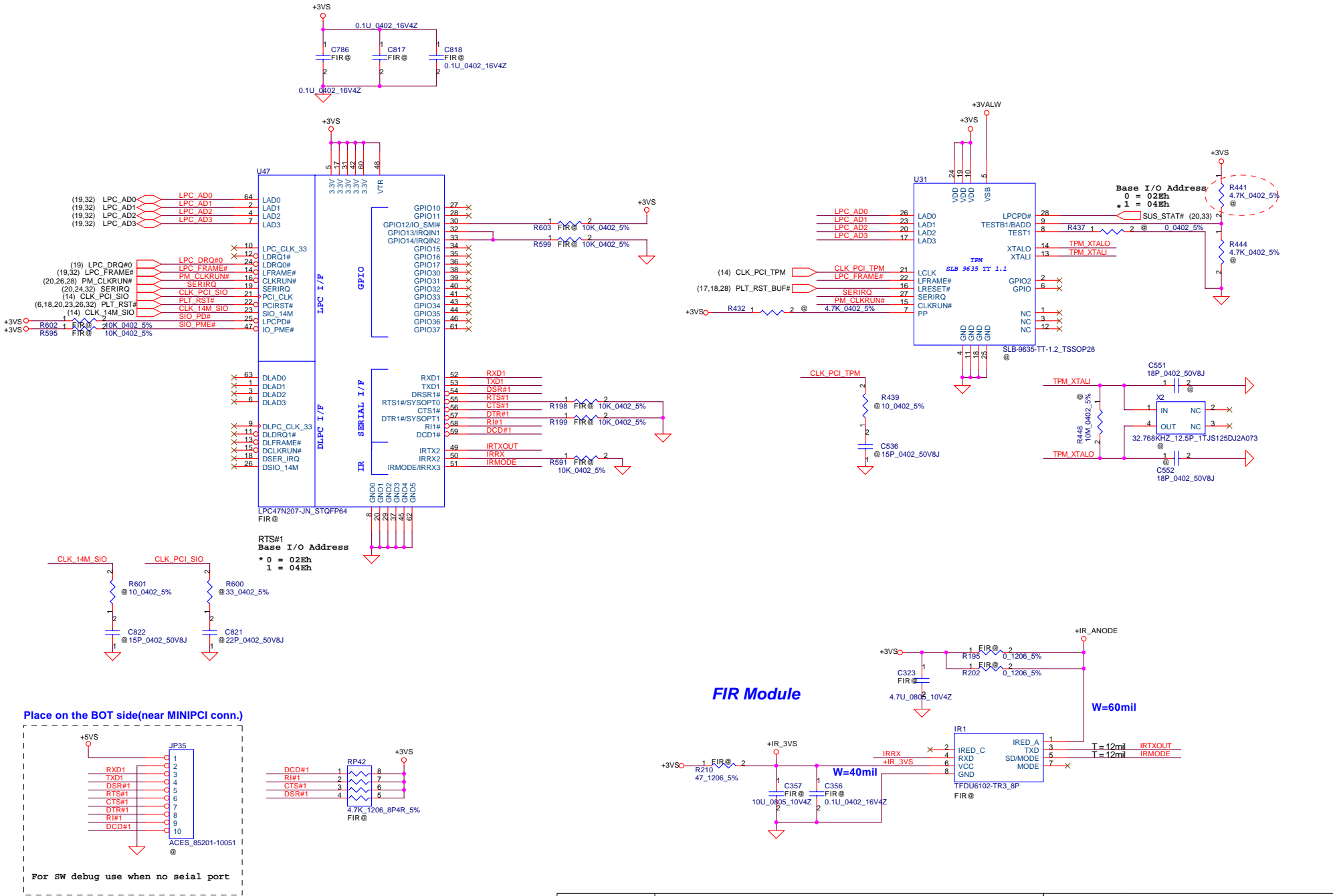
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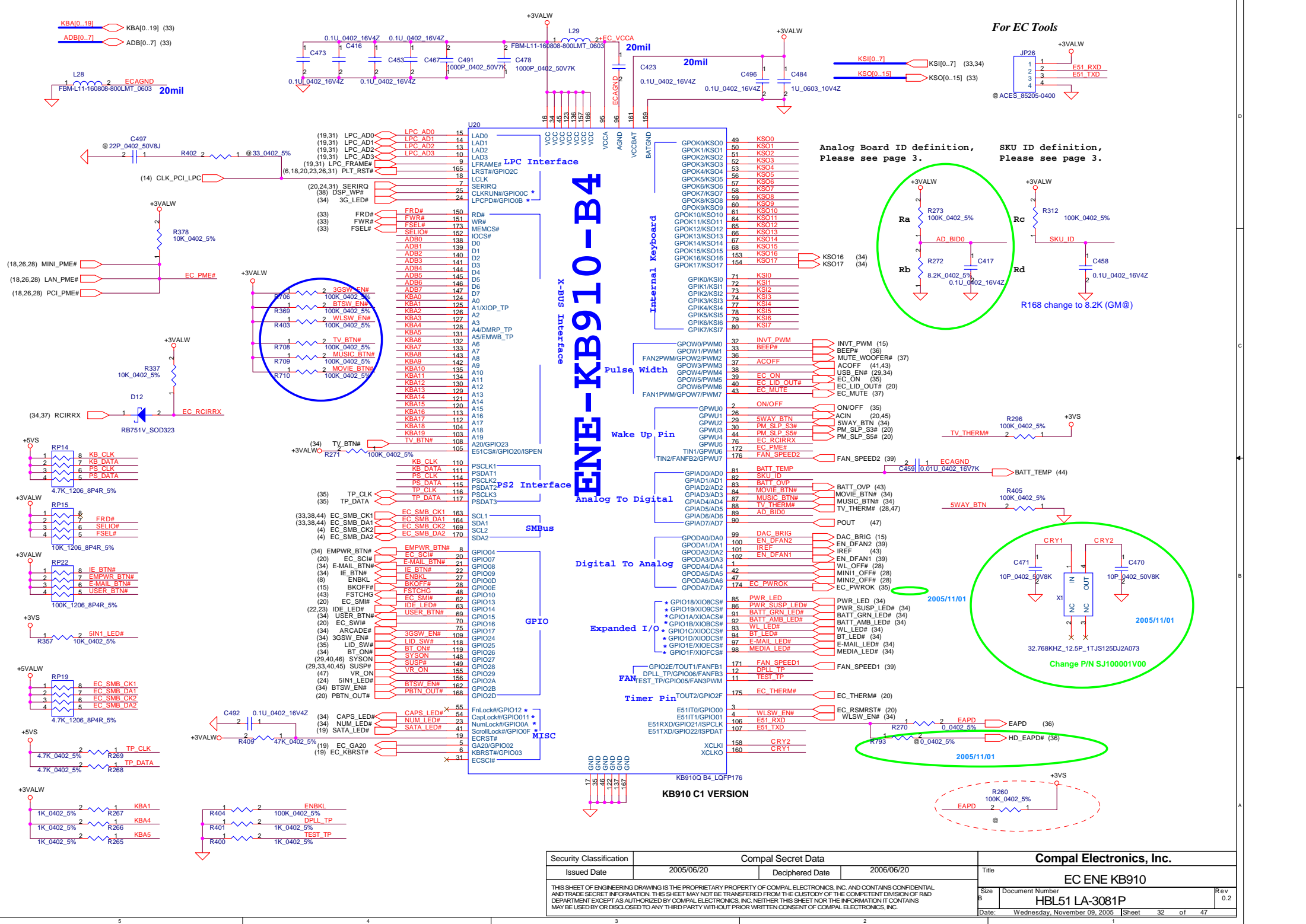




SUPER I/O SMsC LPC47N207



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Size B	Document Number	HBL51 LA-3081P			Rev 0.2	
Date:	Wednesday, November 09, 2005	Sheet	31	of	47	



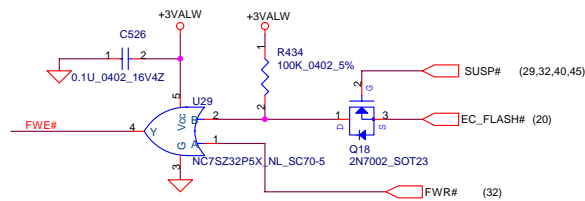
# ENE-KB910-B4

ecvref:sm8-X-bus

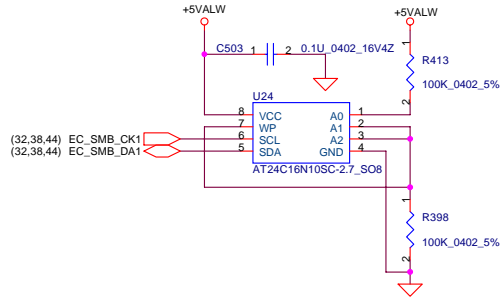
KB910 C1 VERSION

KB910 C1 VERSION

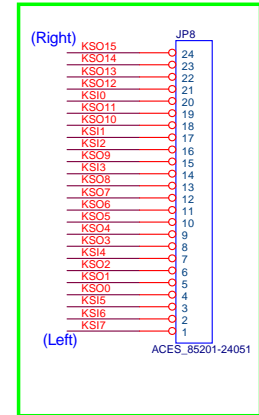
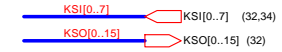
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Size		Document Number		Rev	
B		HBL51 LA-3081P		0.2	
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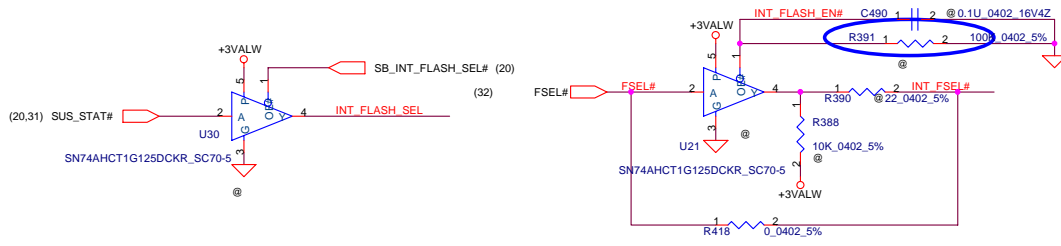
Check PCB Footprint



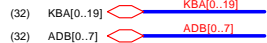
## INT\_KBD Conn.



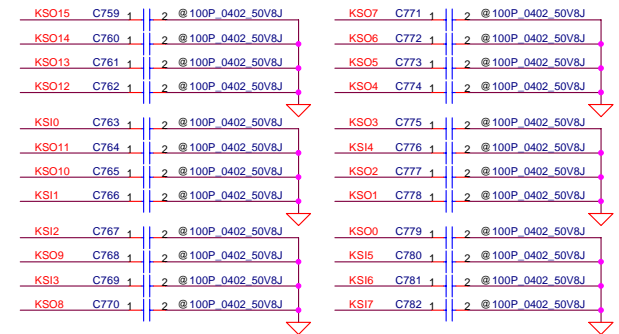
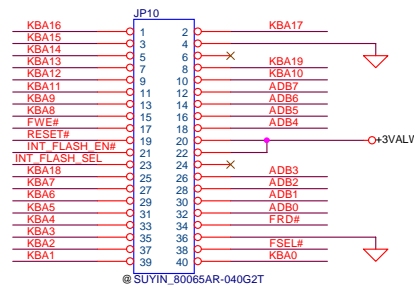
2005/11/03



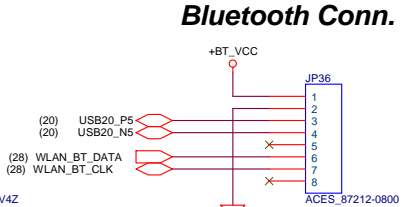
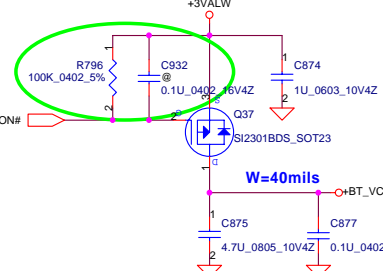
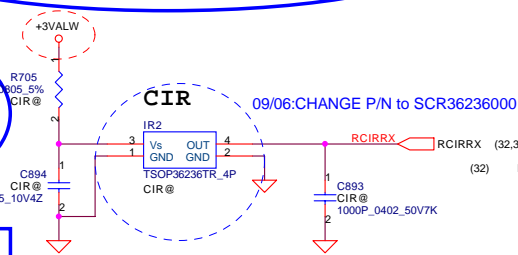
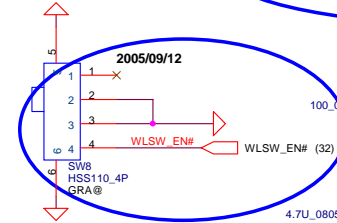
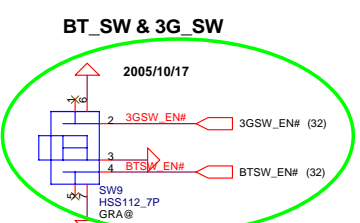
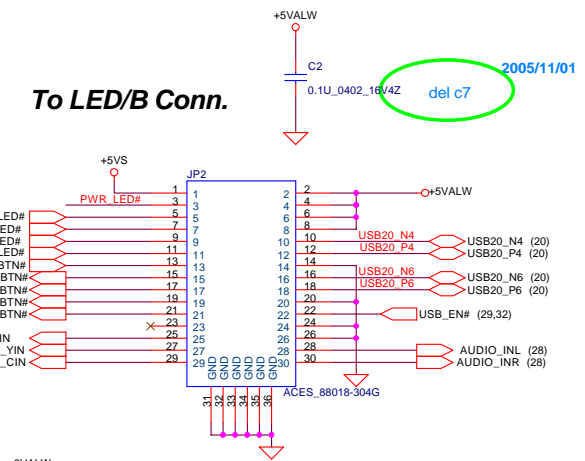
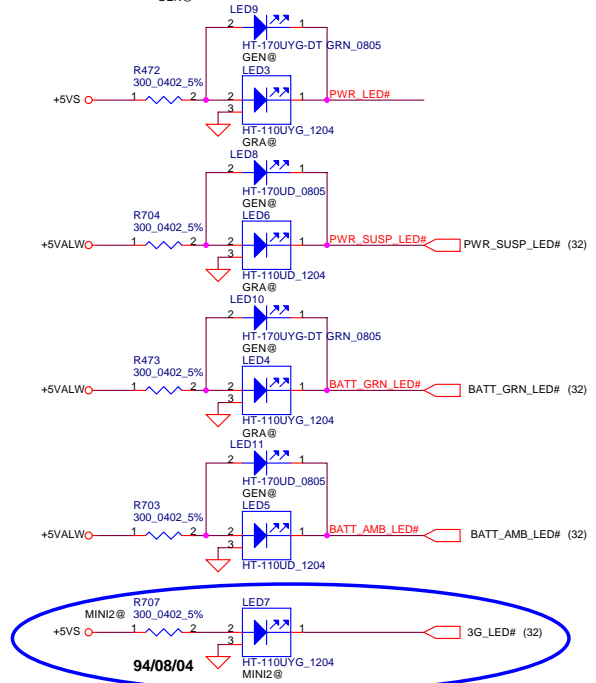
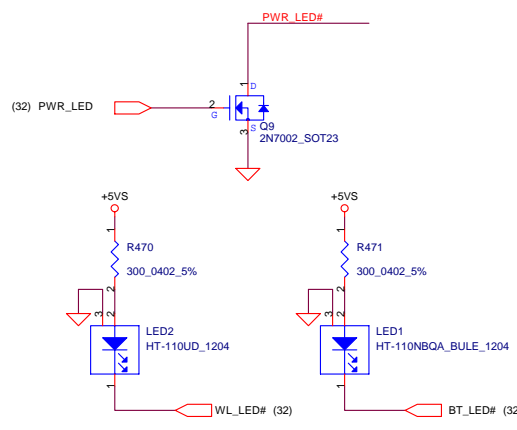
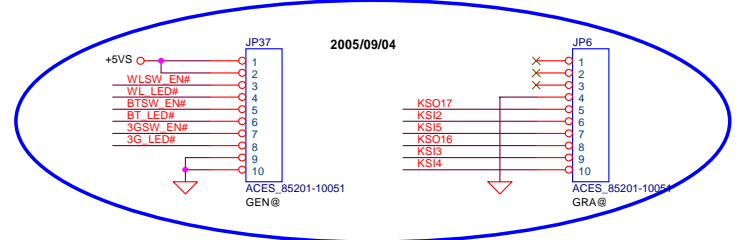
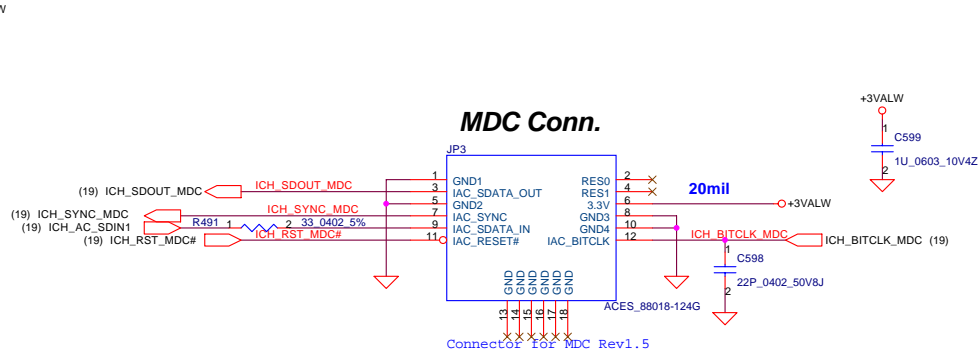
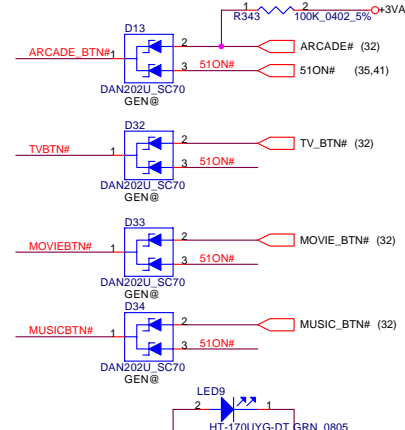
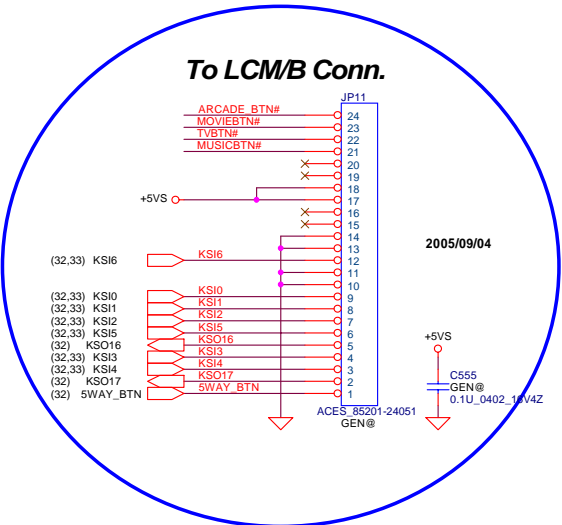
## 1MB Flash ROM



## 1MB ROM Socket

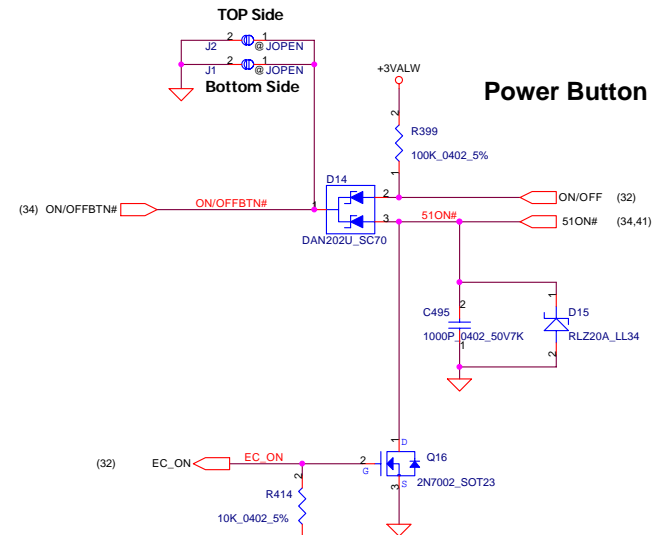


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								Document Number			
								HBL51 LA-3081P			
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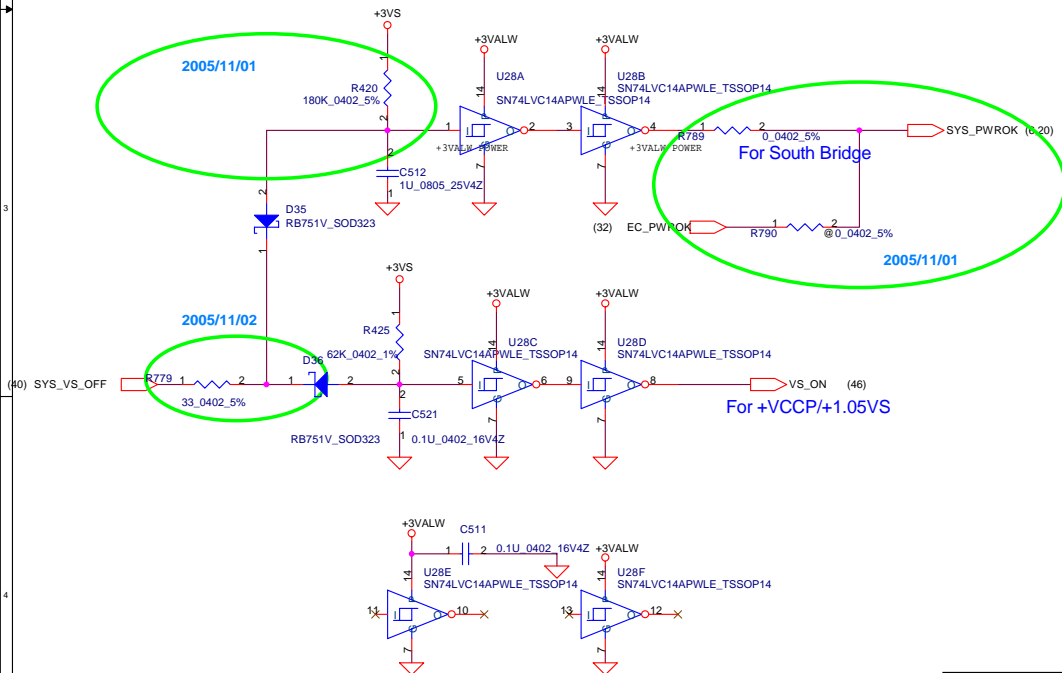


Geneva		Grapevine	
	KSO16	KSO17	
KSI0	VOL_UP	LEFT	
KSI1	RIGHT	VOL_DOWN	
KSI2	PLAY	ENTER	
KSI3	STOP		
KSI4	NEXT		
KSI5	REV		
KSI6		RECORD	

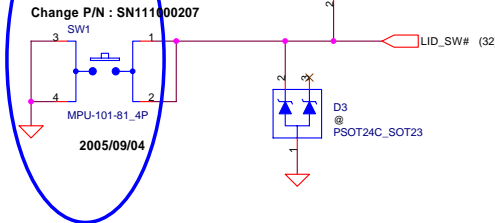
## ON/OFF switch



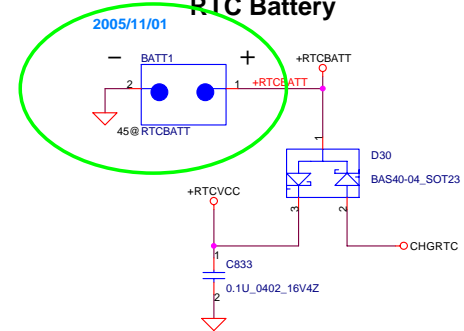
## Power ON Circuit



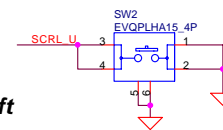
## Lid Switch



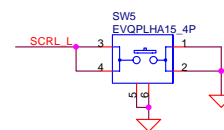
## RTC Battery



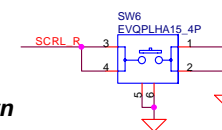
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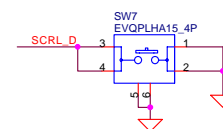
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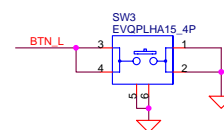
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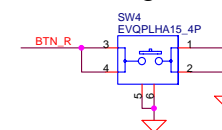
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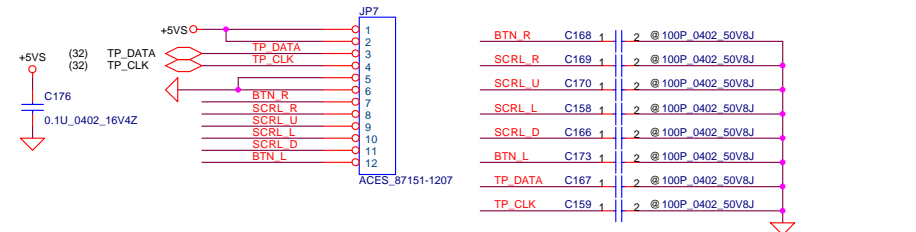
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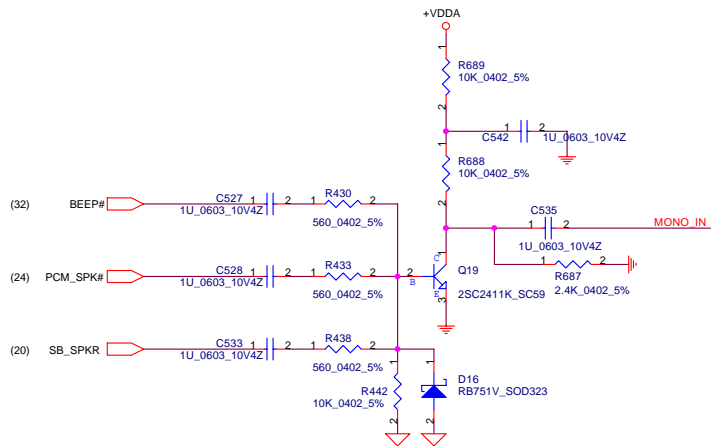
## Right



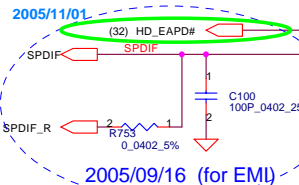
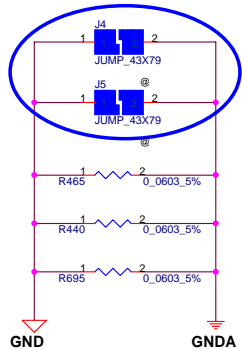
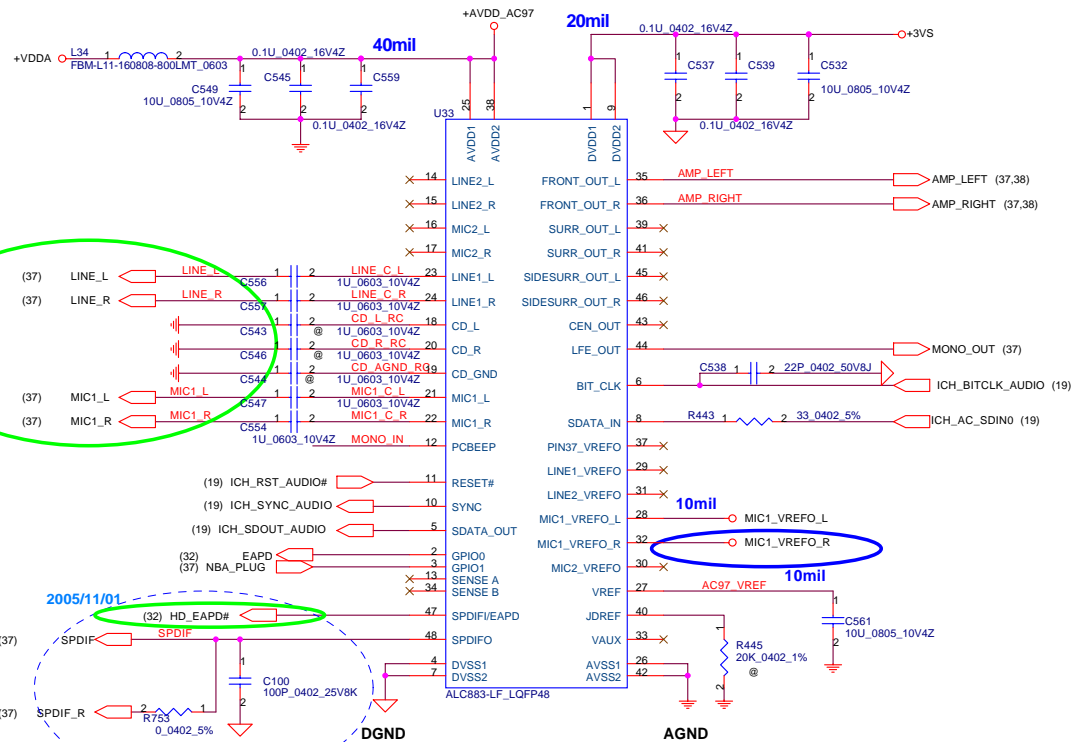
## To TP/B Conn.



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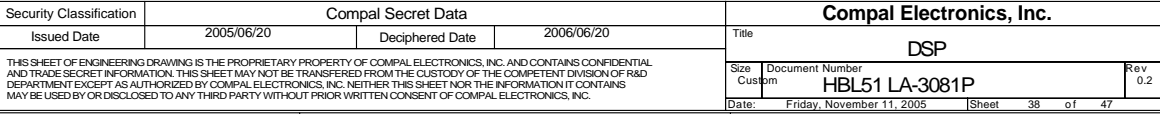
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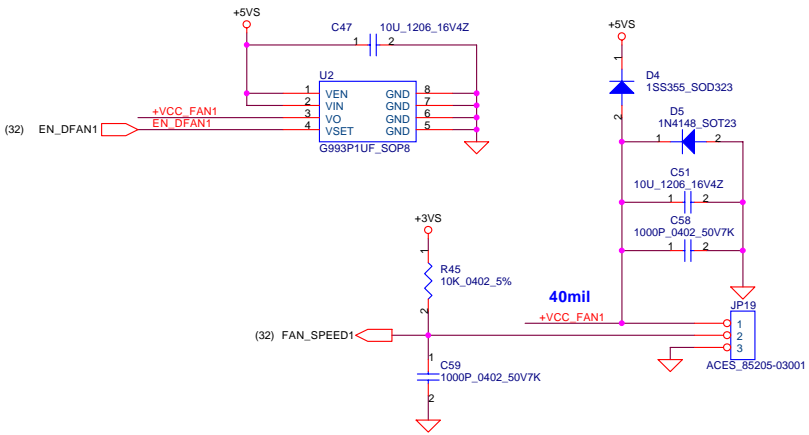
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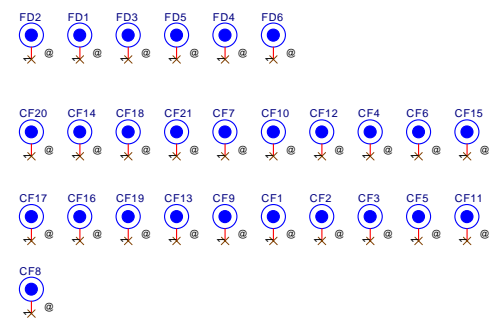
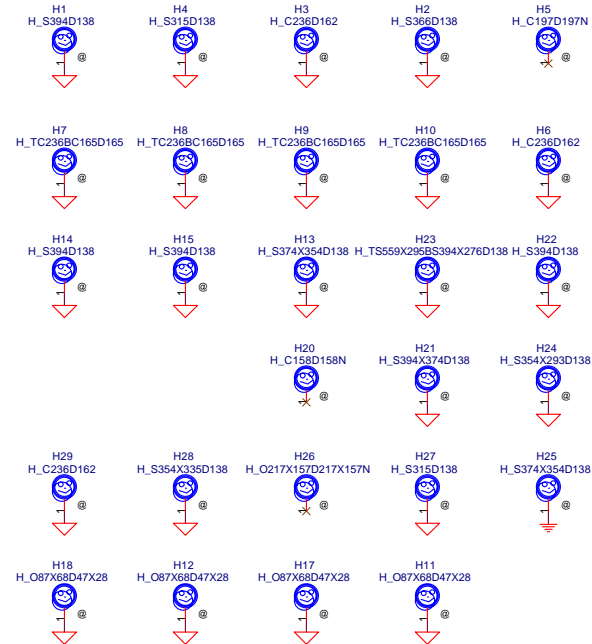
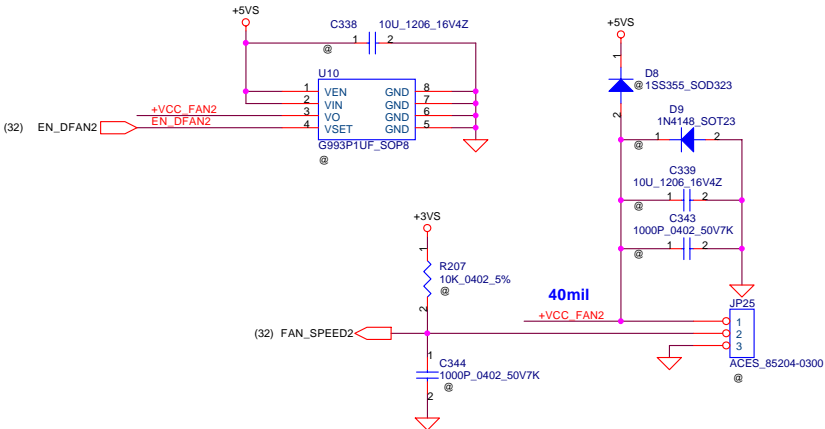




FAN1 Conn

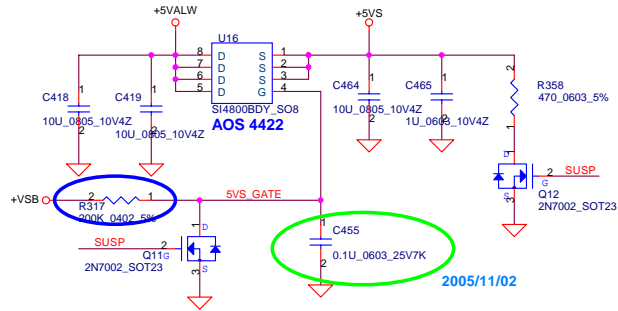


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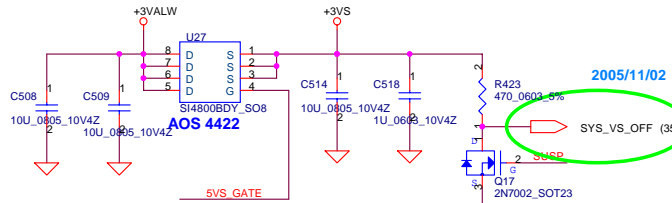


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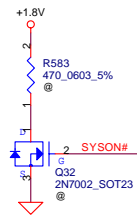
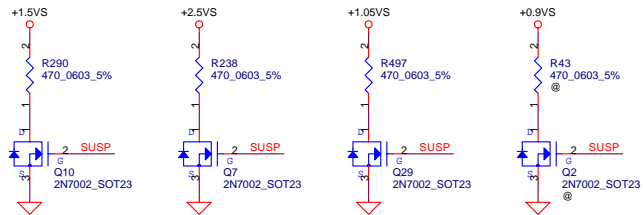
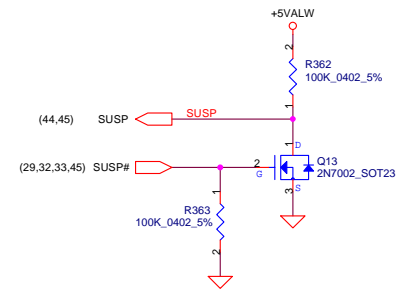
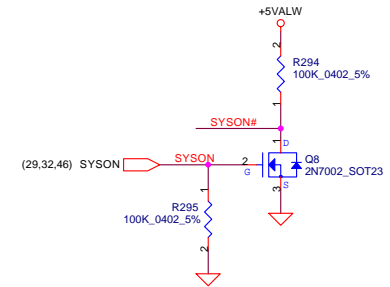
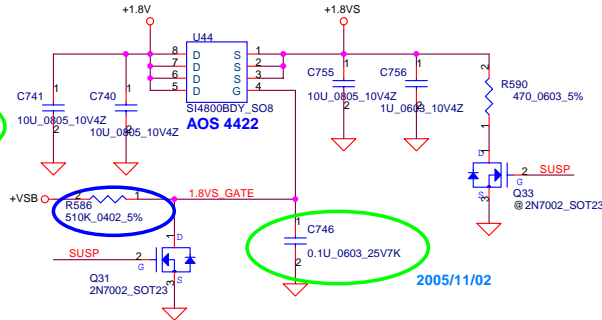
# **+5VALW TO +5VS**



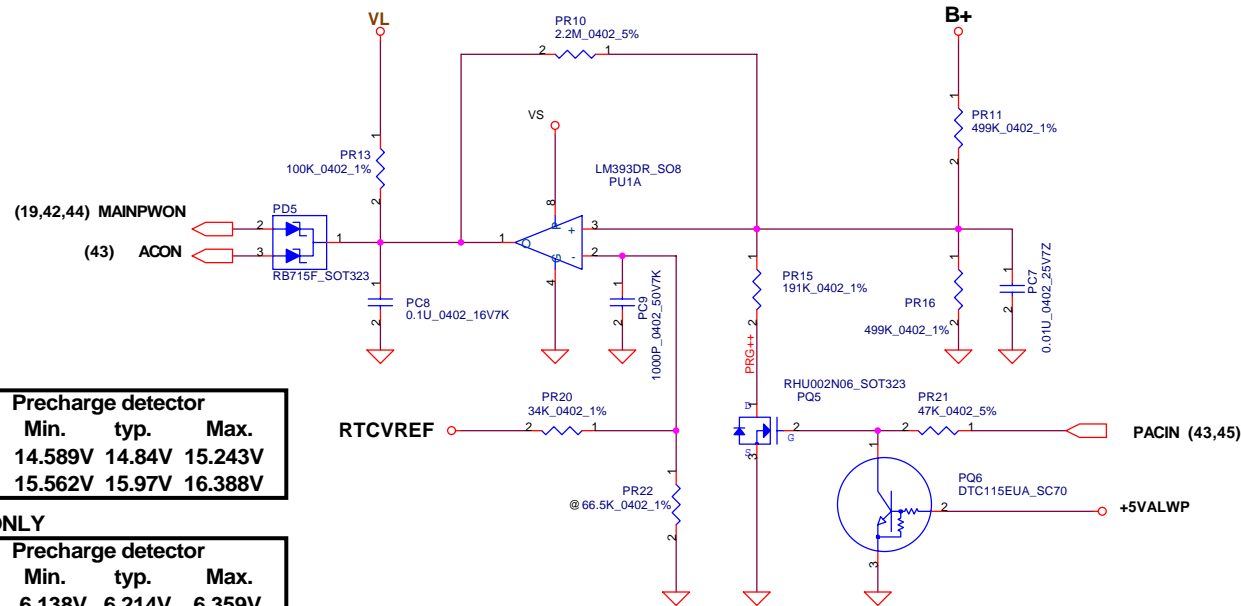
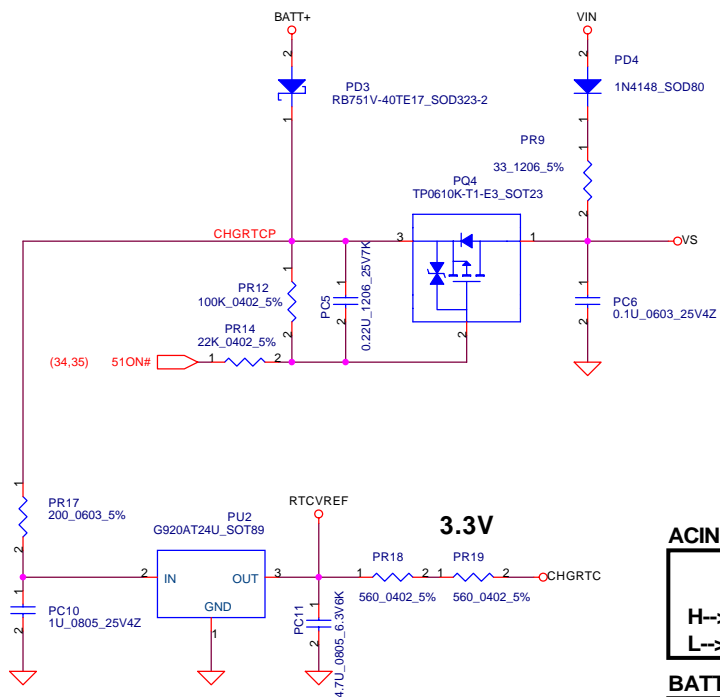
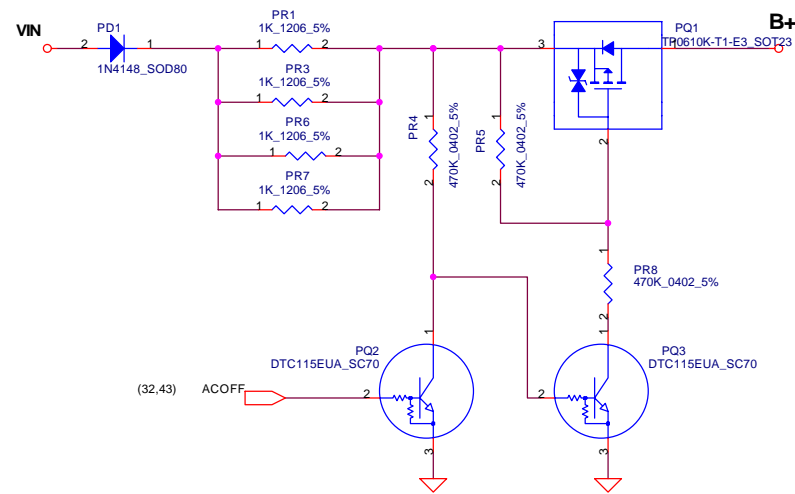
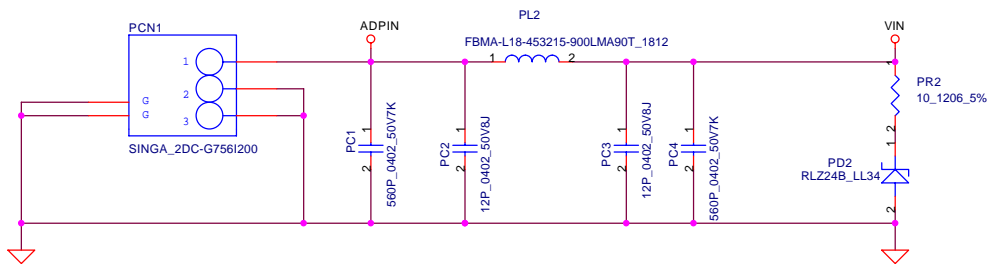
# **+3VALW TO +3VS**



# **+1.8V to +1.8VS**



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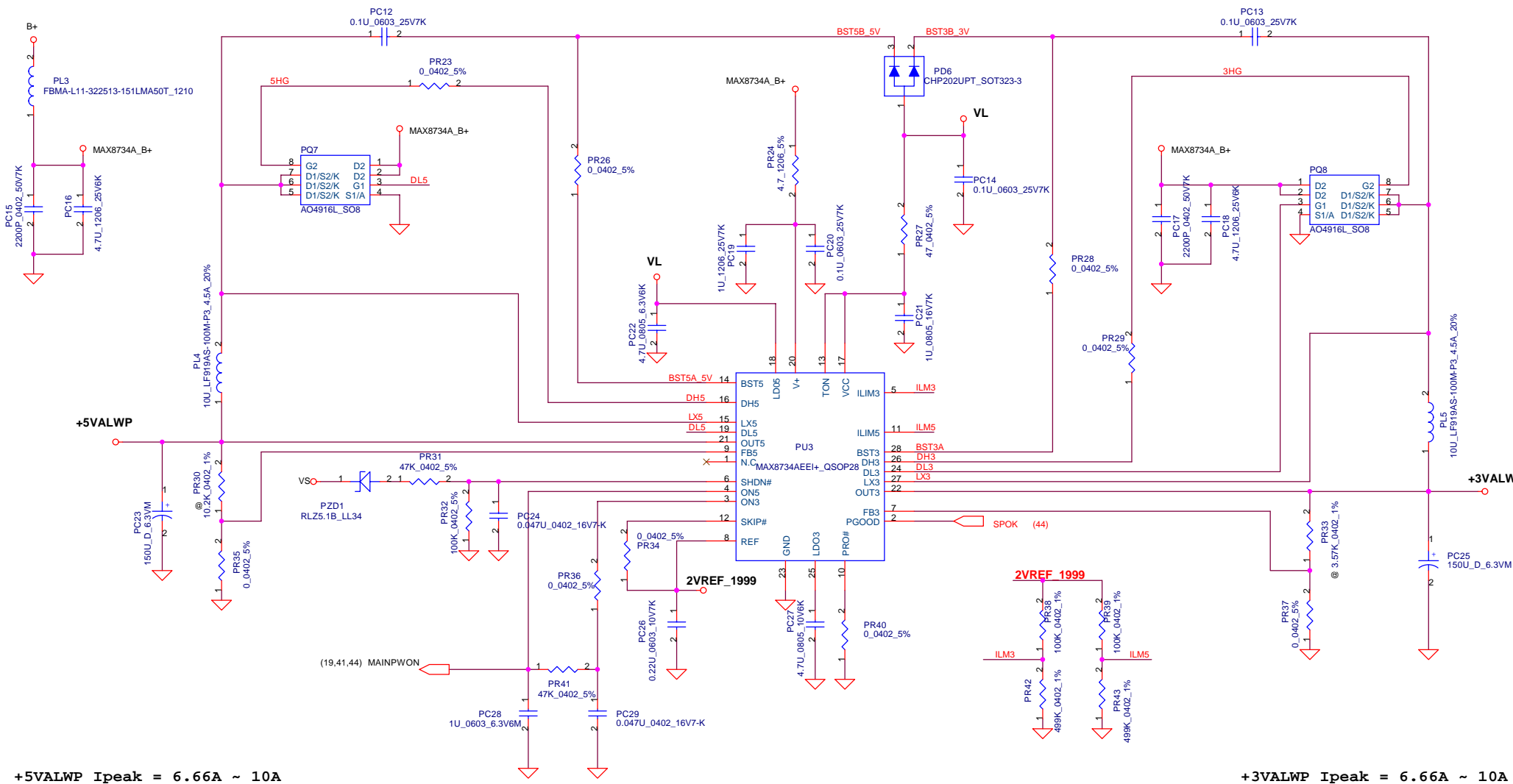


ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

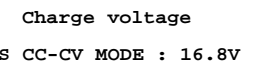
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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				Size	Document Number
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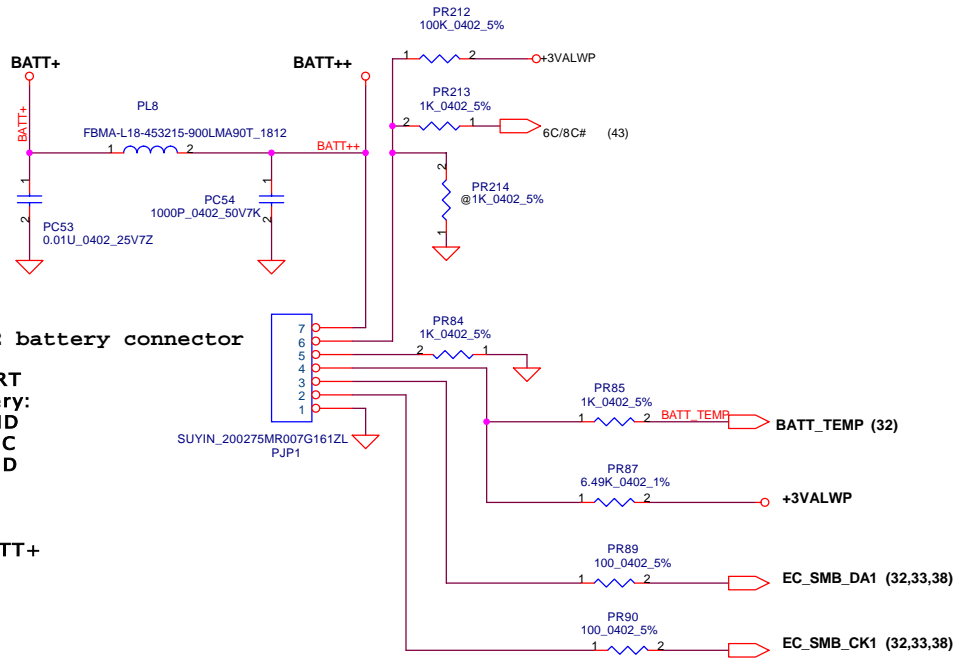


```
OVP voltage :
LI-3S :17.8V----BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+
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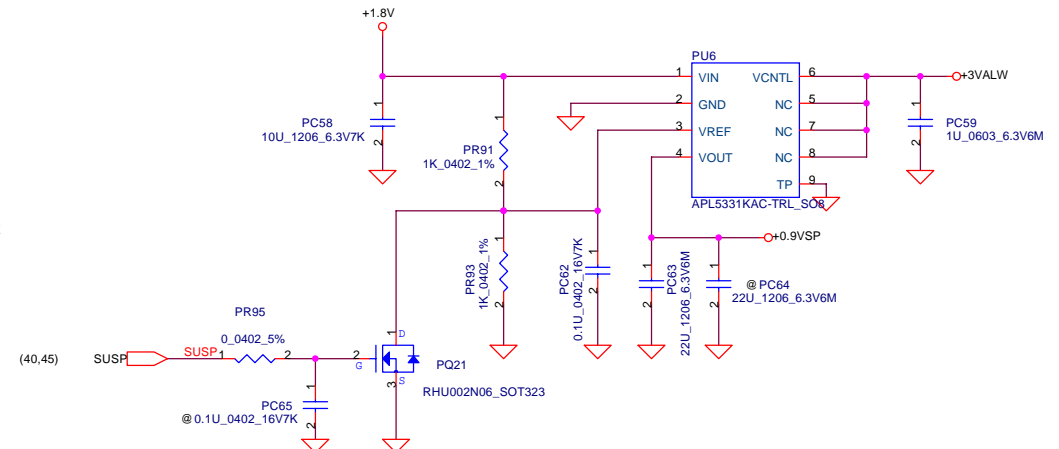
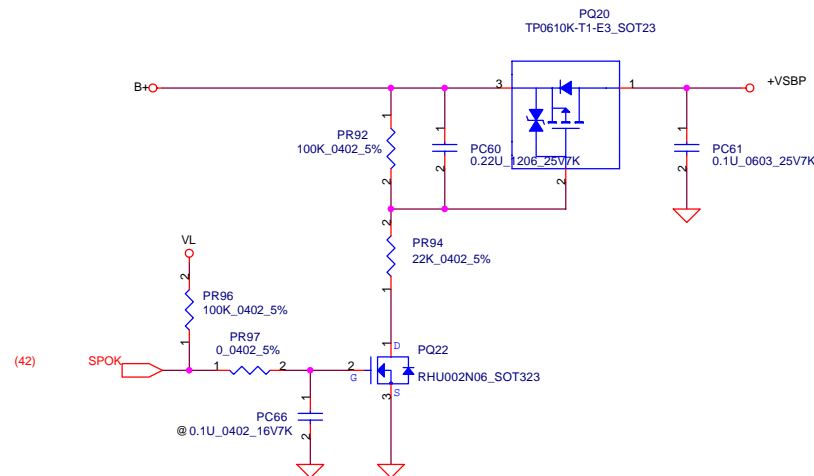
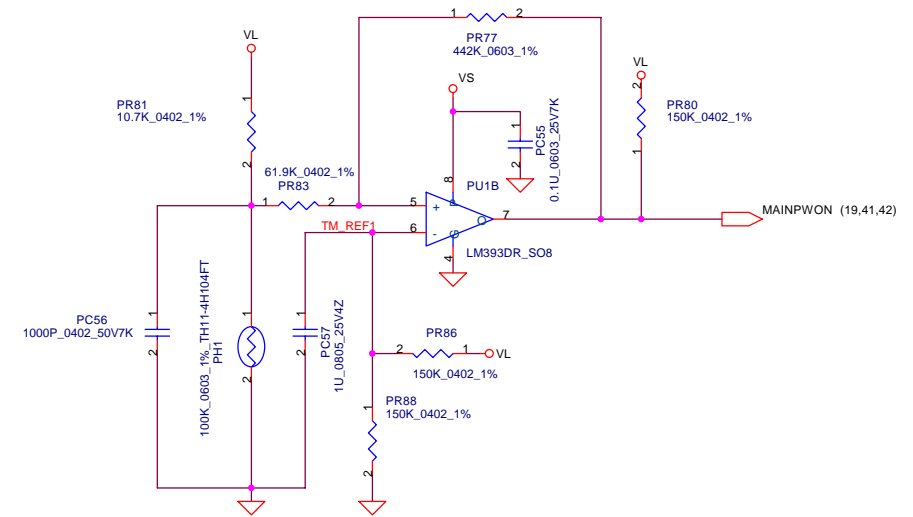
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Charger			
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# PJP2 battery connector

**SMART Battery:**  
 1.GND  
 2.SMC  
 3.SMD  
 4.TS  
 5.B/I  
 6.ID  
 7.BATT+



**PH1 under CPU bottom side :**  
 CPU thermal protection at 80 degree C  
 Recovery at 44(45) degree C

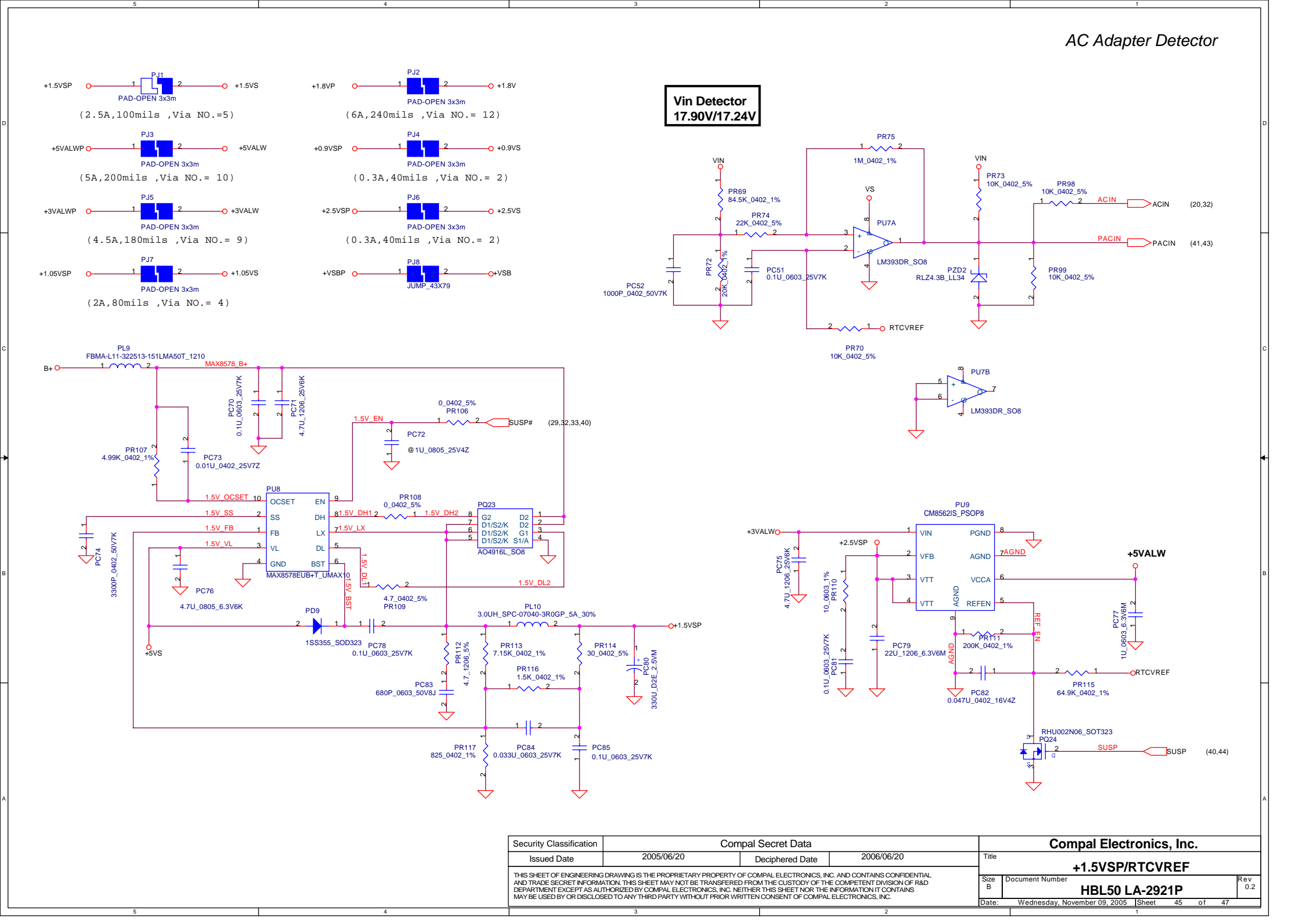
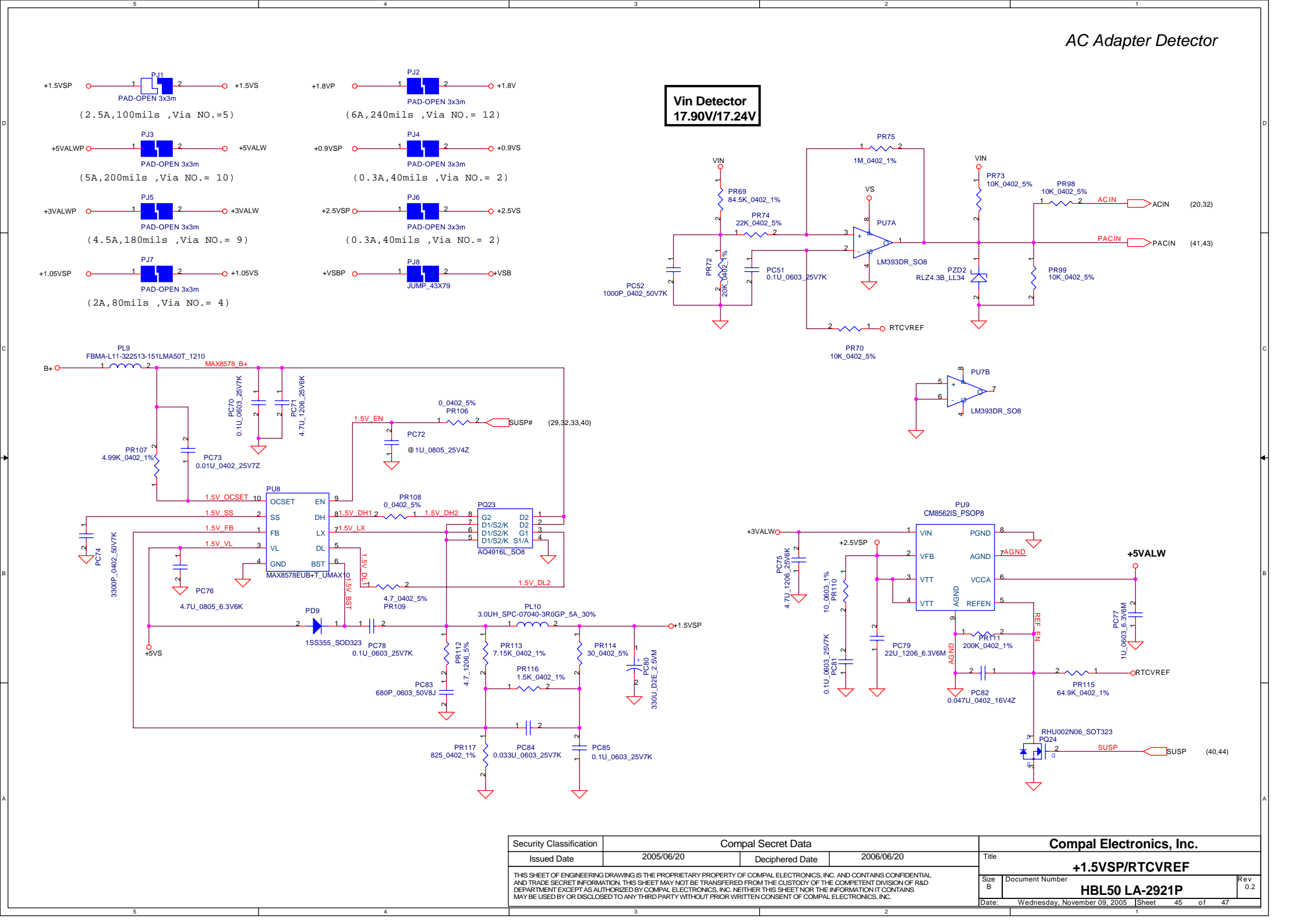
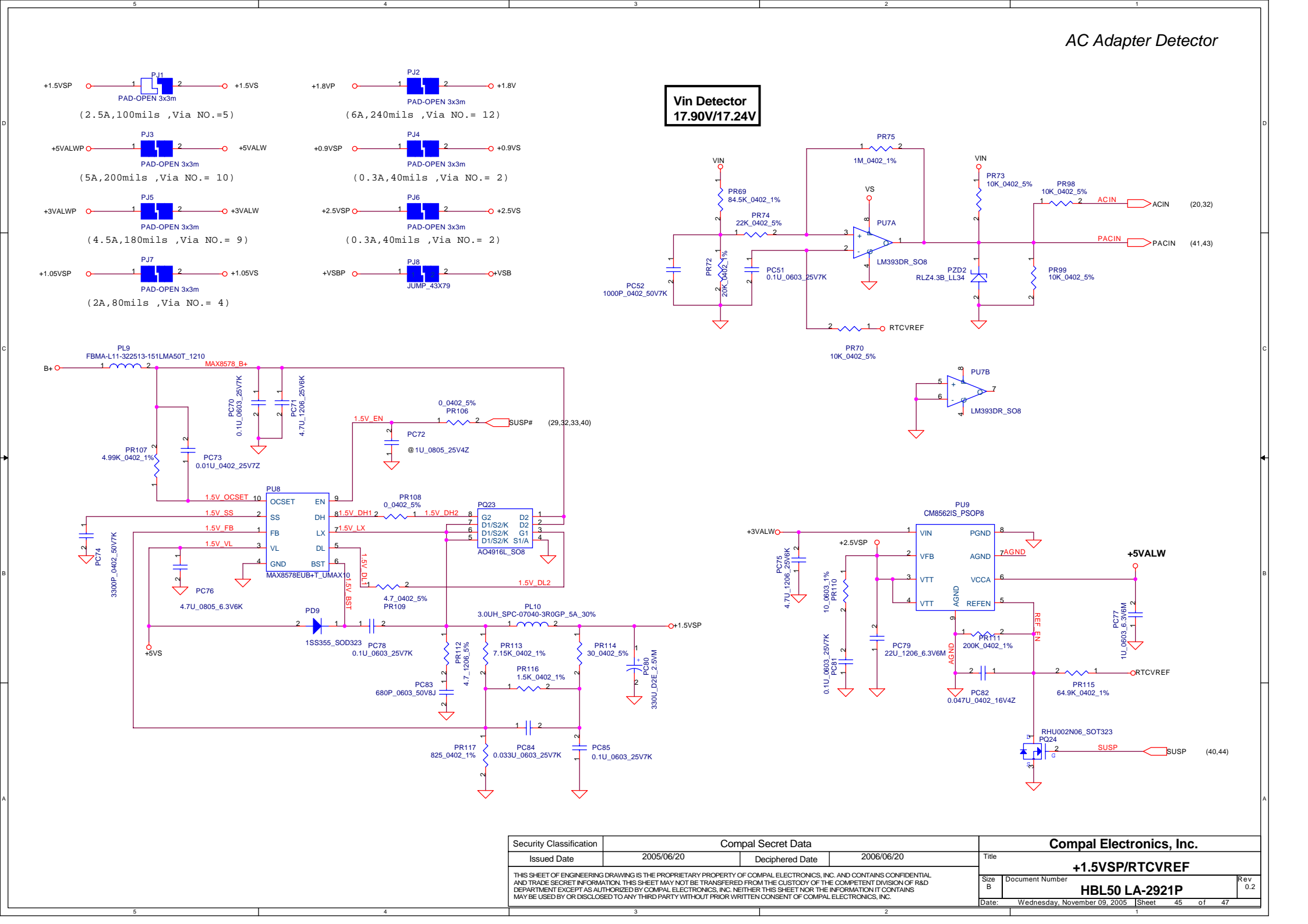
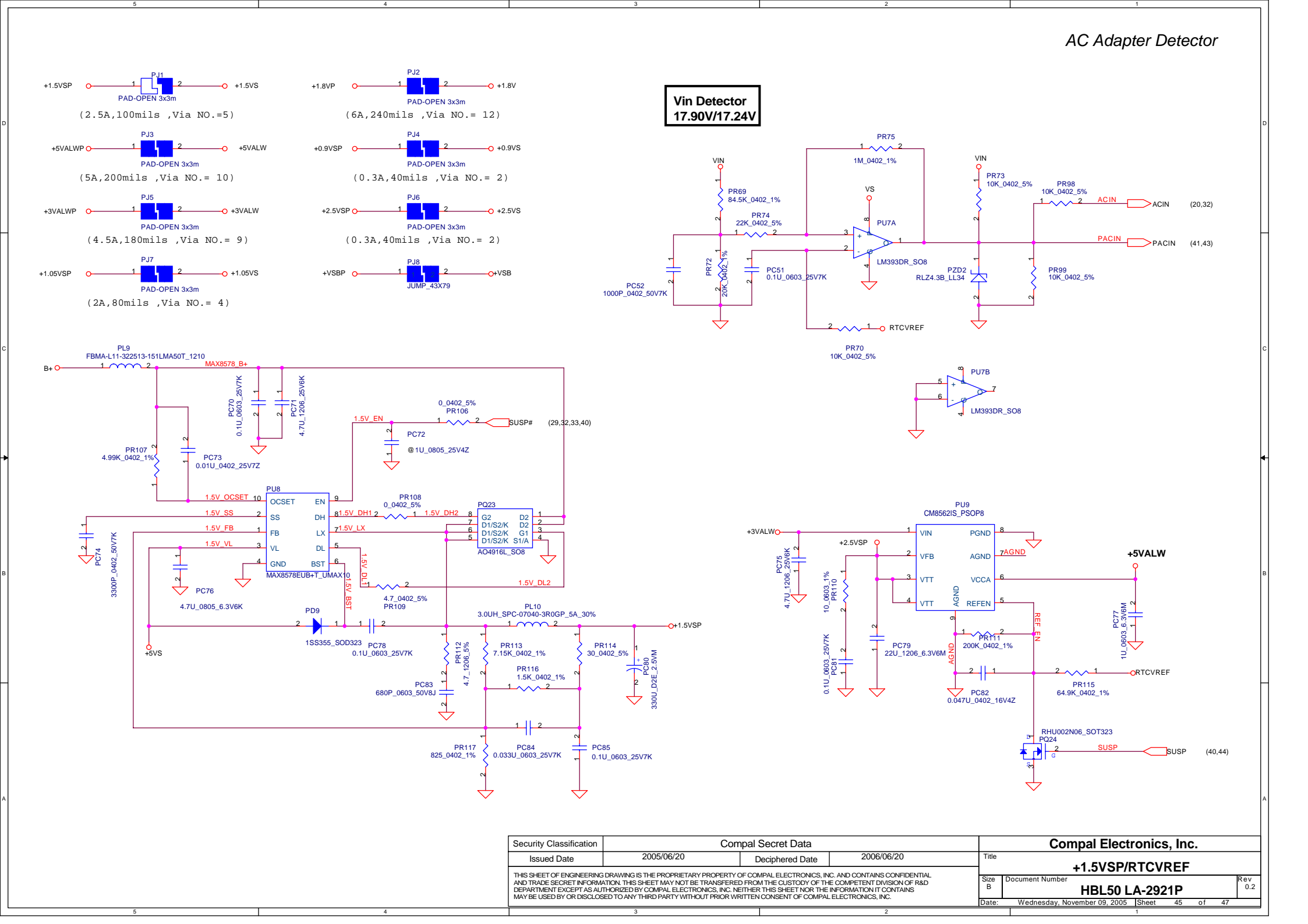


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# AC Adapter Detector

## Vin Detector 17.90V/17.24V

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