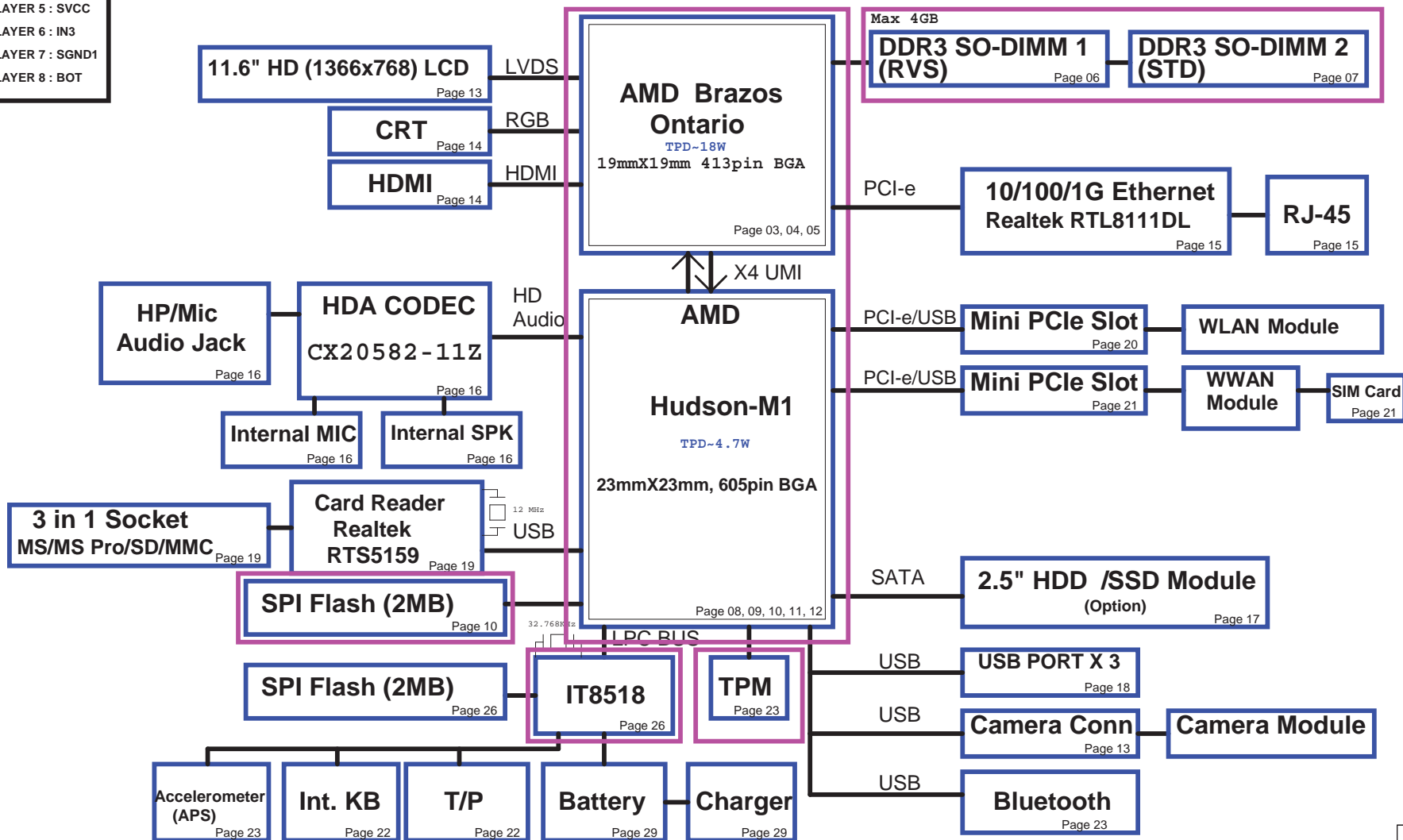


LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT




POWER

DC/DC 3V_PCU, 5V_PCU, +15V	Page 30
REGULATOR (DDR3) 1.5V_SUS, 0.75V_DDR_VTT	Page 31
REGULATOR +1V	Page 32
REGULATOR 1.1V_S5, +1.1V	Page 33
REGULATOR +1.8V	Page 34
CPU Core	Page 35
RUN POWER SW 3V_SUS, 5V_SUS, 3V_S5, 5V_S5 +3V, +5V	Page 36
Discharge	Page 36

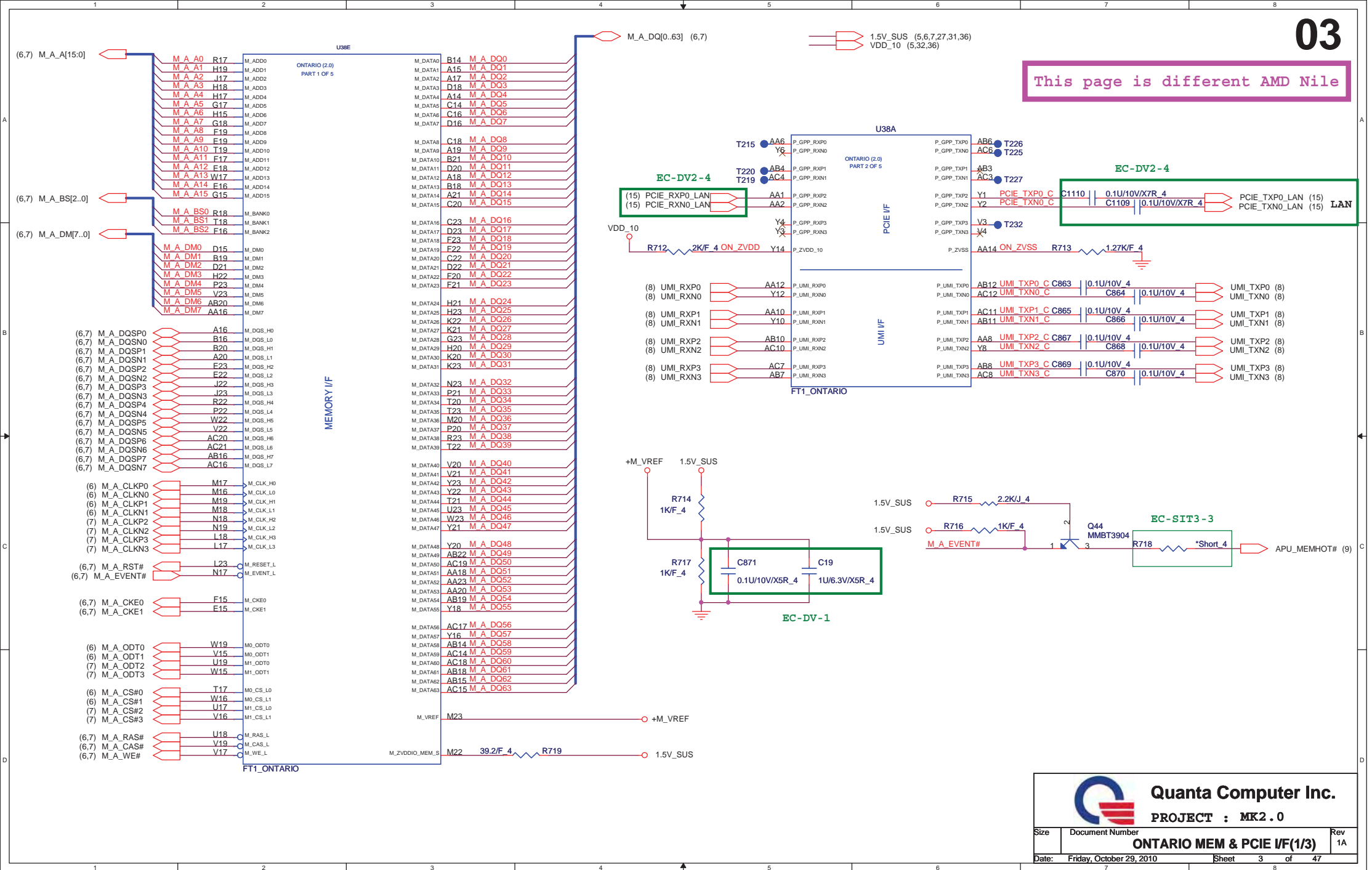
Power Sequence



KBC(EC) SM BUS

 Quanta Computer Inc. PROJECT : MK2.0		
Size	Document Number	Rev
	System Information	1A
Date:	Friday, October 29, 2010	Sheet 2 of 47

This page is different AMD Nile



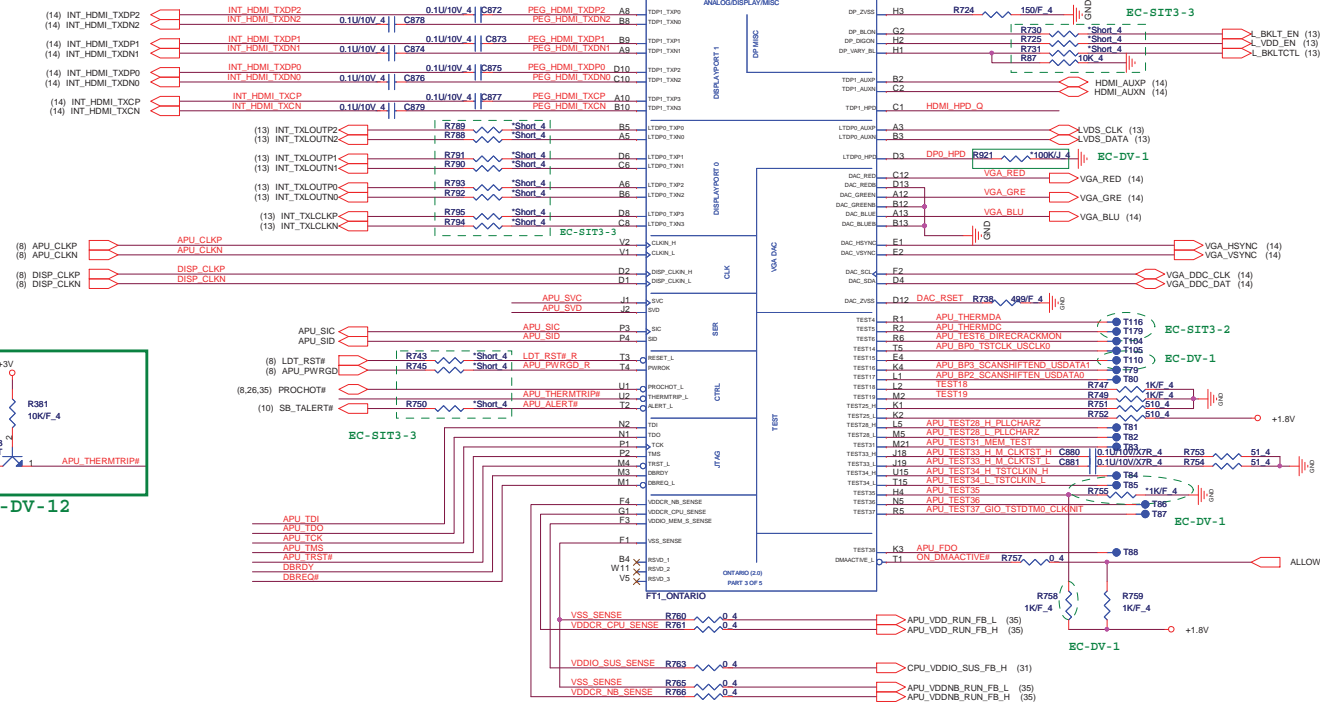
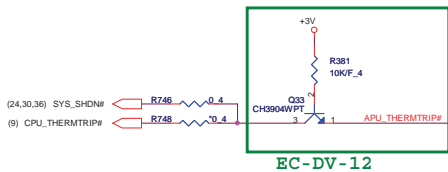
Quanta Computer Inc.

PROJECT : MK2.0

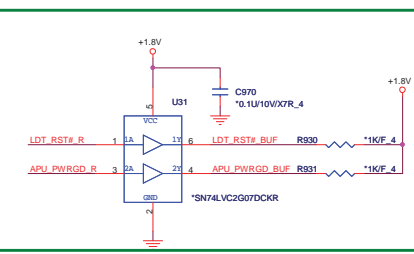
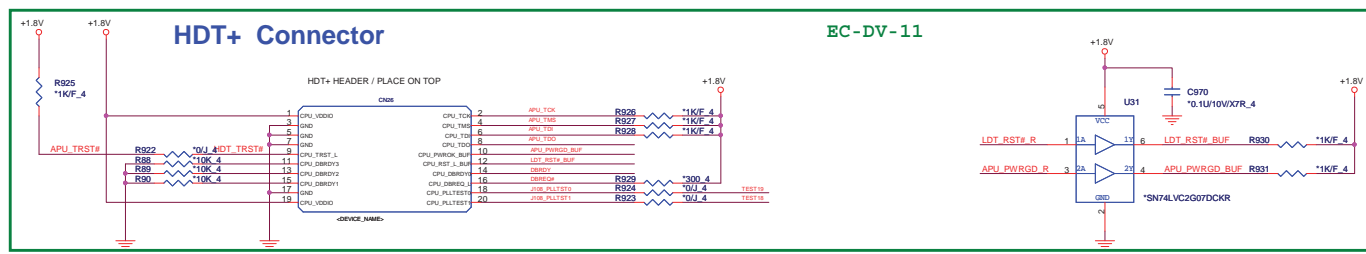
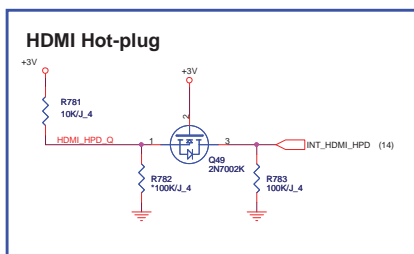
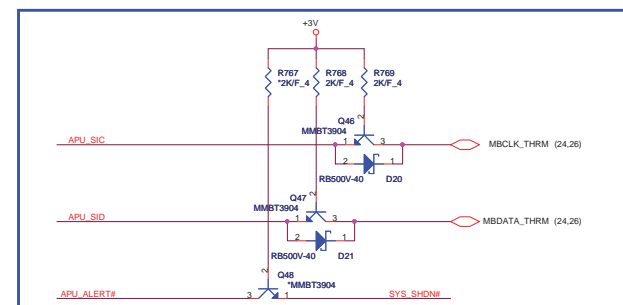
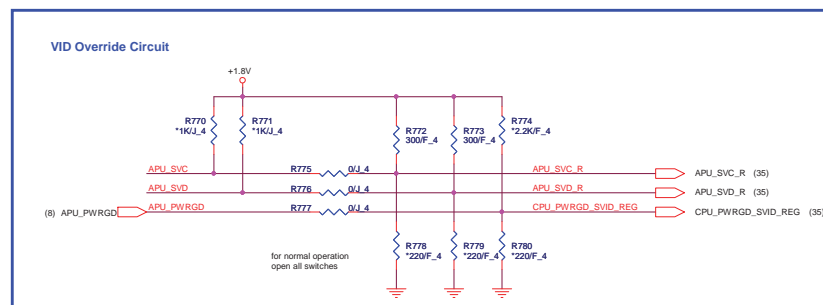
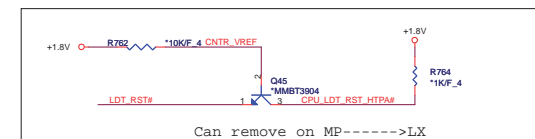
Size	Document Number	Rev
	ONTARIO MEM & PCIe I/F(1/3)	1A

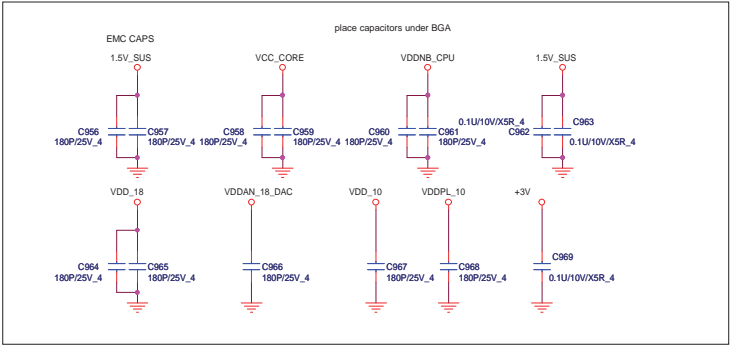
Date: Friday, October 29, 2010 Sheet 3 of 47

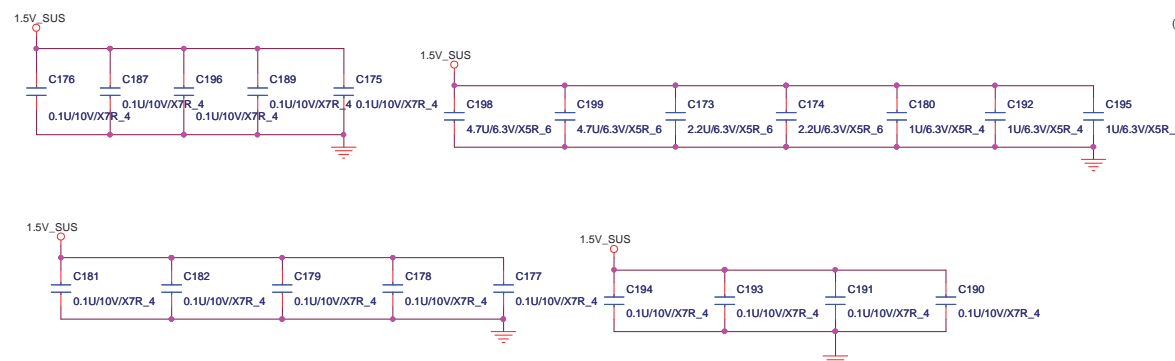
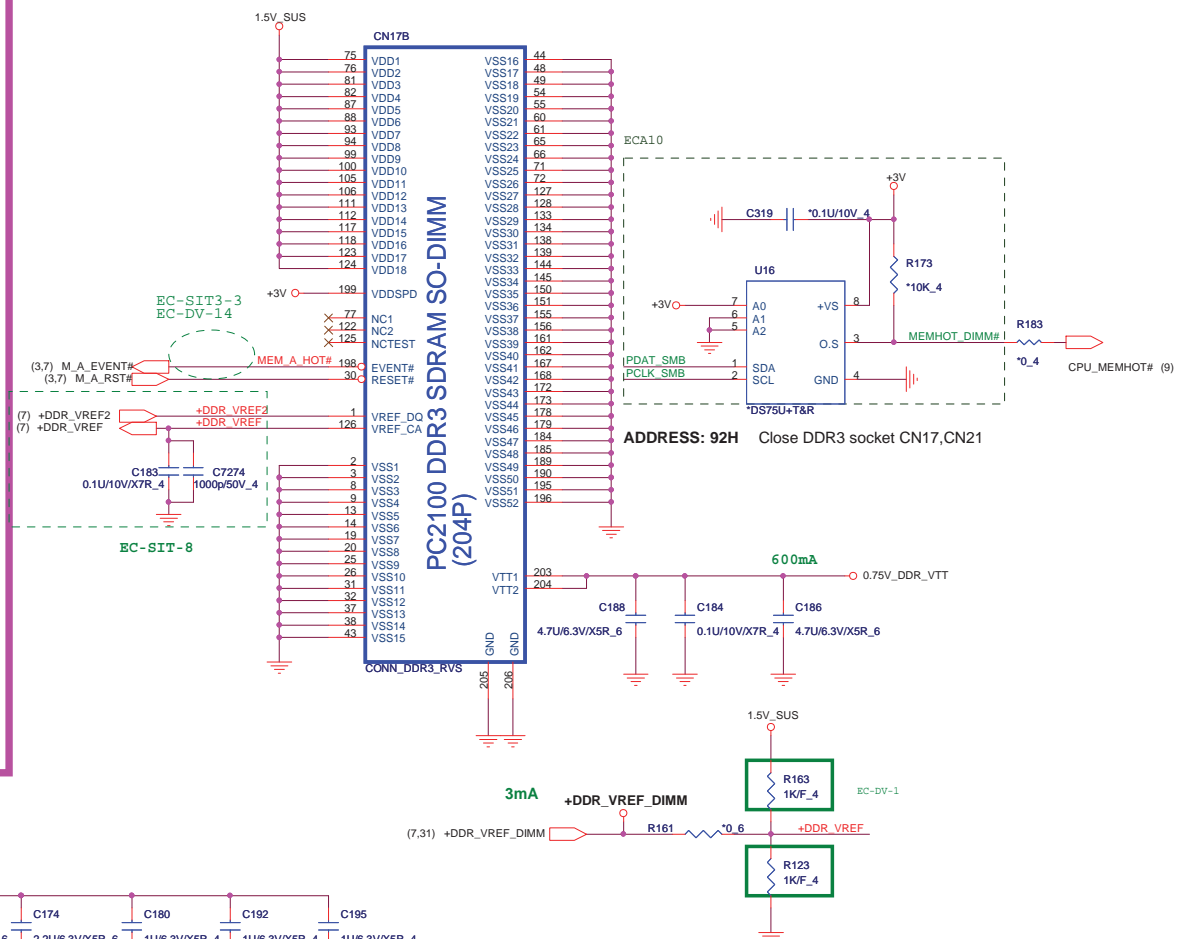
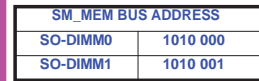
This page is different AMD Nile

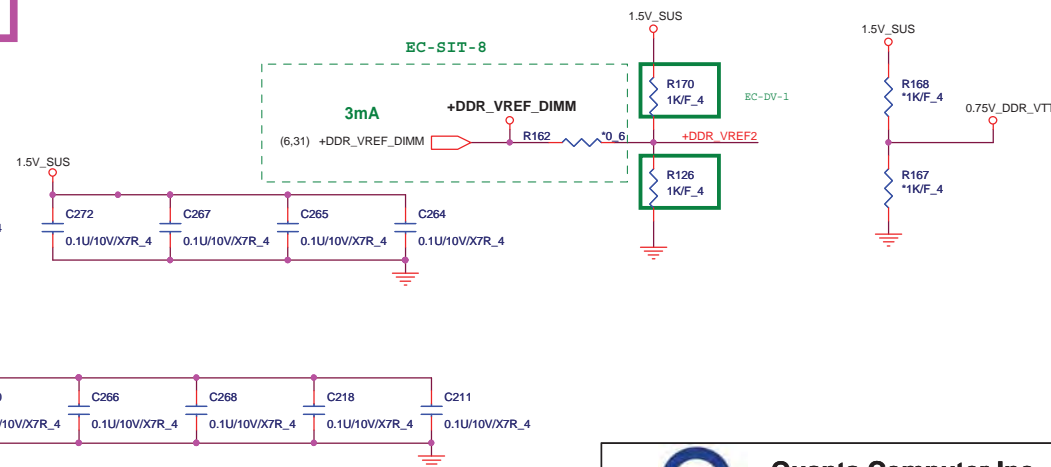
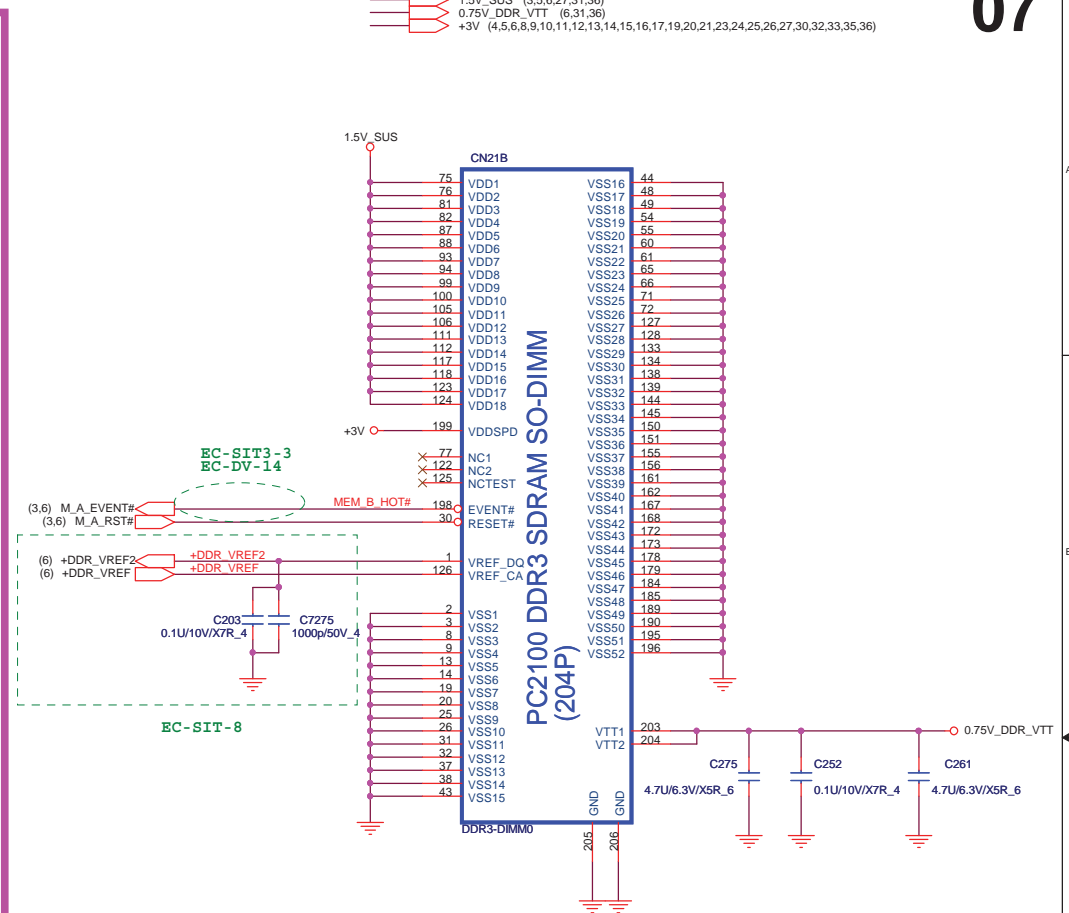


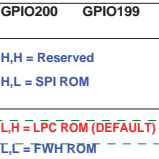
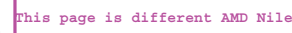
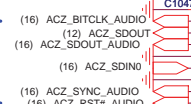
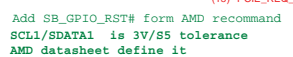
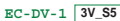
DIFFERENTIAL ROUTING









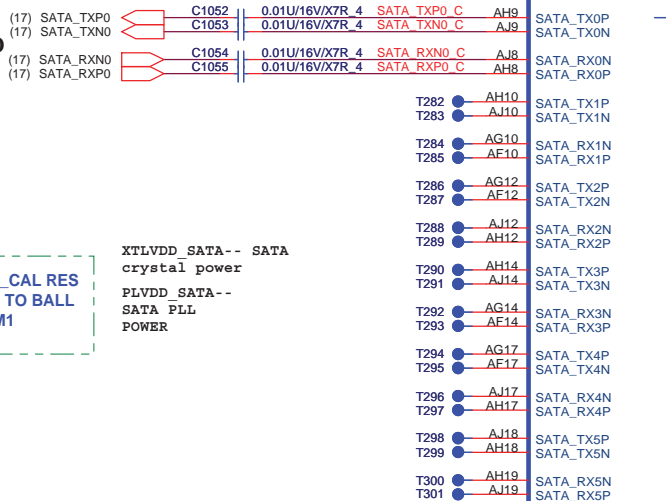




```
SATA PORT 0,1,2,3
can support AHCI
mode
```

PLACE SATA AC COUPLING
CAPS CLOSE TO Hudson M1

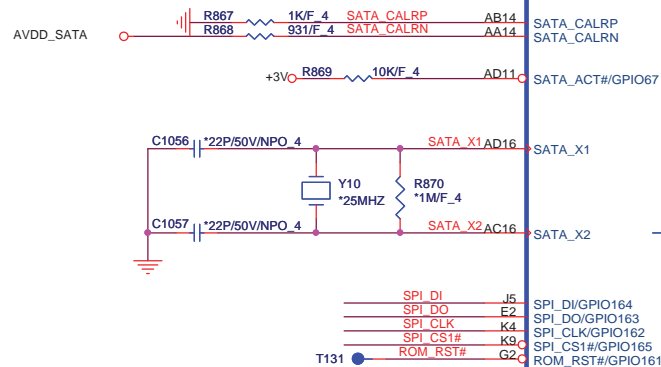
SATA HDD



PLACE SATA_CAL RES
VERY CLOSE TO BALL
OF Hudson M1

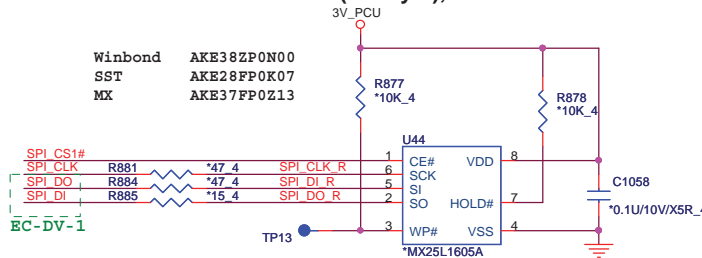
```
XTLVDD_SATA-- SATA
crystal power

PLVDD_SATA--
SATA PLL
POWER
```

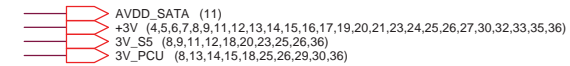
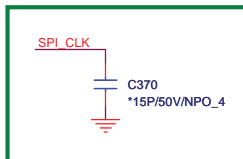


EC-SIT-14

16Mbit (2M Byte), SPI

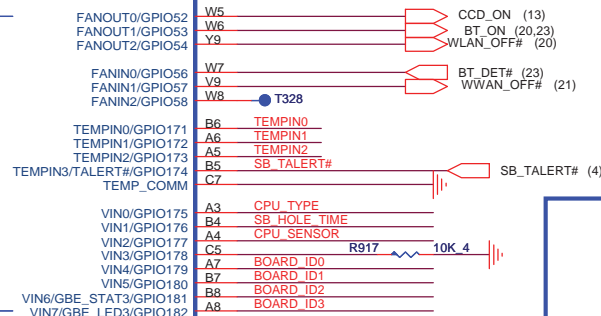
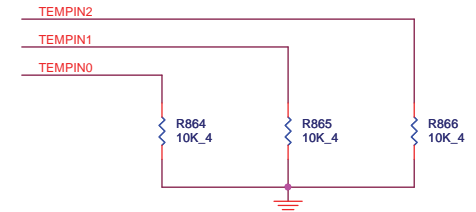


EC-DV-2 RF Suggest



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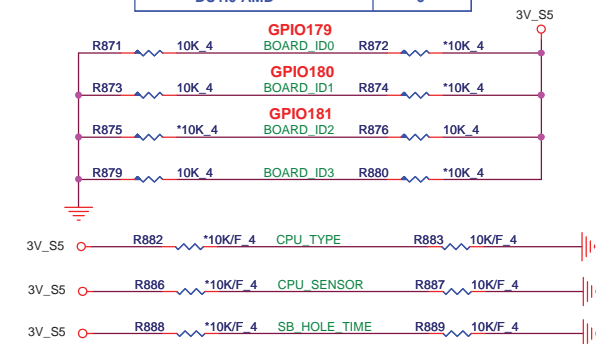
AMD recommend : TEMPIN0 / TEMPIN1 / TEMPIN2
can not maintain on floating stages when without usage.
Do not care pull high or pull down.



CPU THERMAL	GPIO179
External	1
SB-TSI	0

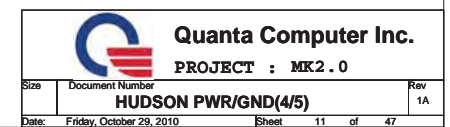
SB8XX Hold Time	GPIO180
1.2V	1
1.1V	0

DU1/MK2	GPIO181
MK2.0 AMD	1
DU1.0 AMD	0

**Quanta Computer Inc.**

PROJECT : MK2.0

Size	Document Number HUDSON SATA/BID_s(3/5)	Rev 1A
Date:	Friday, October 29, 2010	Sheet 10 of 47

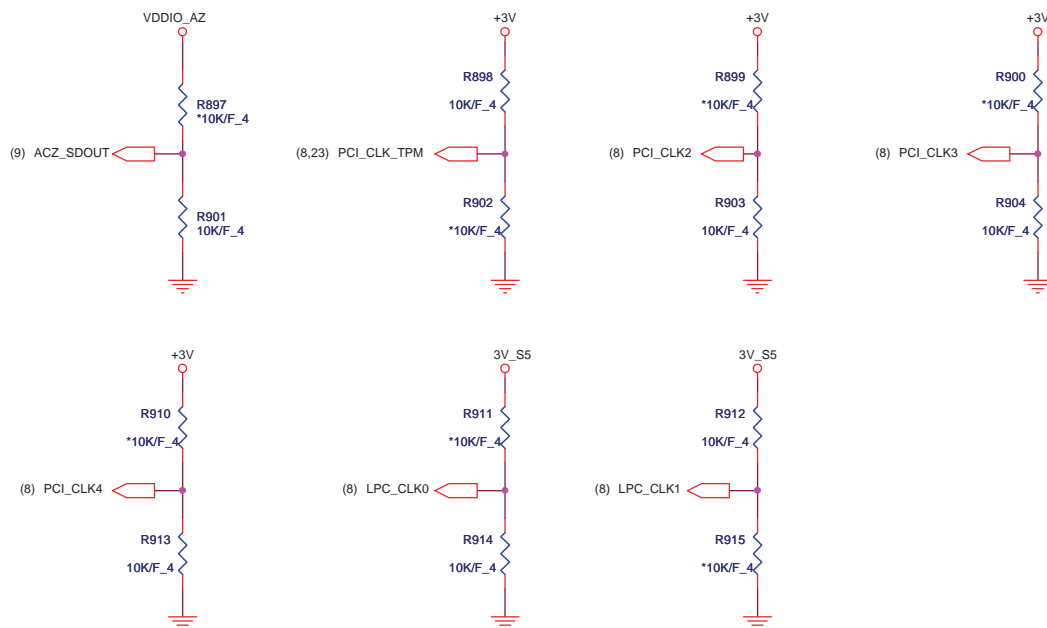




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

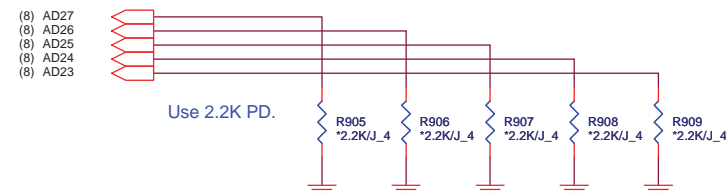
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

VDDIO_AZ (11)
+3V (4,5,6,7,8,9,10,11,13,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)
3V_S5 (8,9,10,11,18,20,23,25,26,36)

12

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



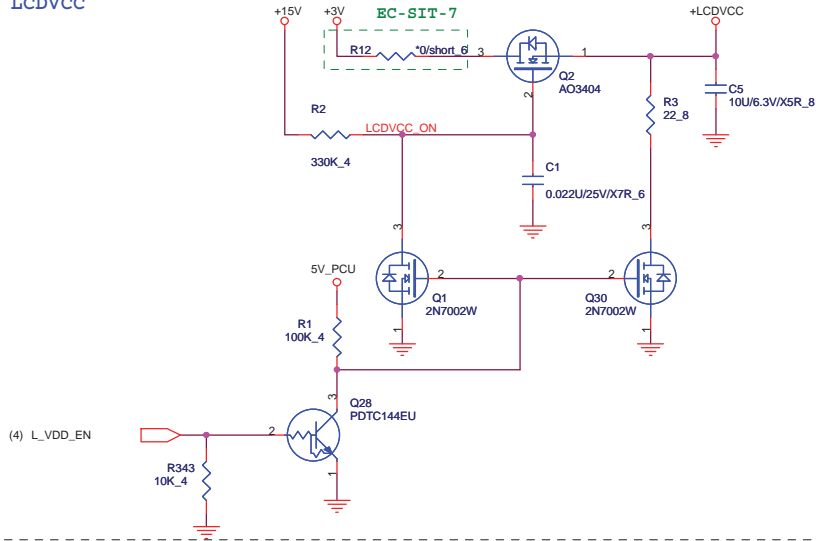
Quanta Computer Inc.

PROJECT : MK2.0

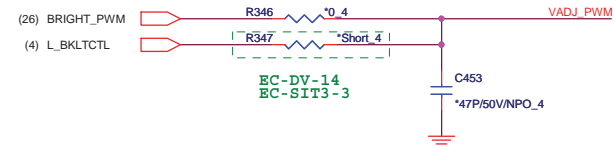
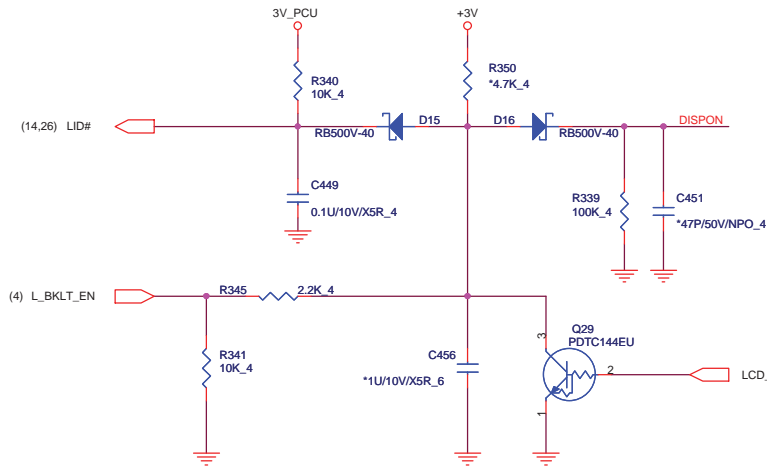
Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	1A
Date:	Friday, October 29, 2010	Sheet 12 of 47

+3V (4,5,6,7,8,9,10,11,12,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)
 3V_PCU (8,10,14,15,18,25,26,29,30,36)
 +15V (23,30,33,36)
 +5V (14,16,17,22,24,26,27,36)
 VIN (29,30,31,32,33,35,36)
 5V_SUS (25,32,34,35,36)
 5V_PCU (27,29,30,31,33,36)

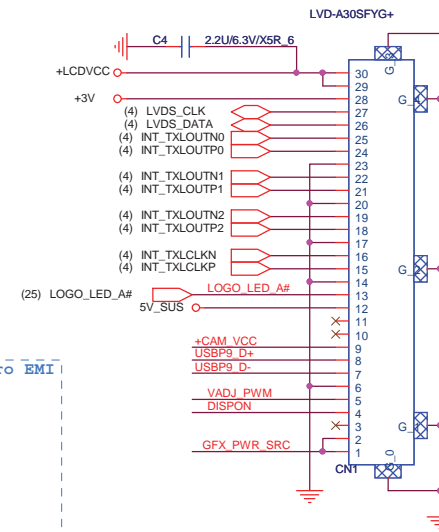
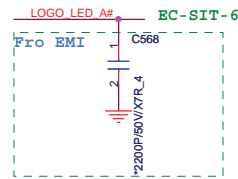
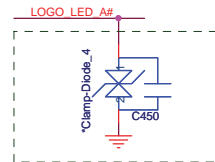
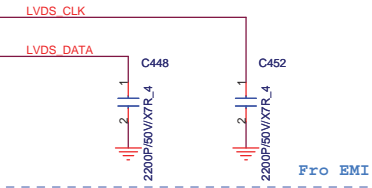
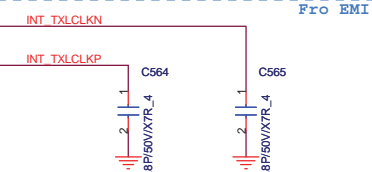
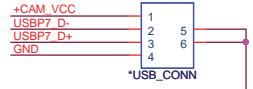
LCDVCC



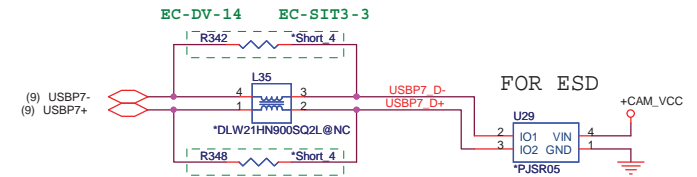
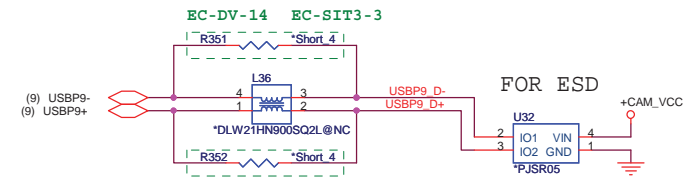
Back light



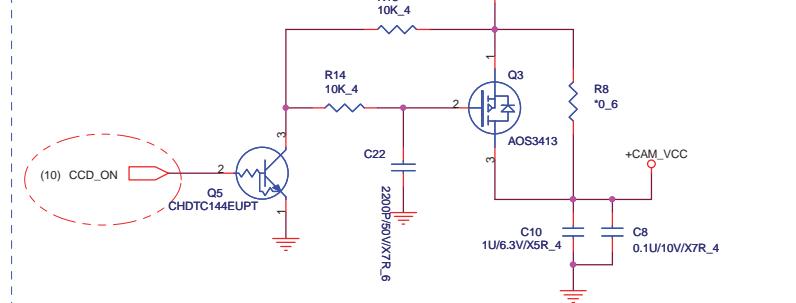
EC-DV2-1



LVDS (11.6")
 (1024x600,
 1366x768)



CAMERA VCC Control

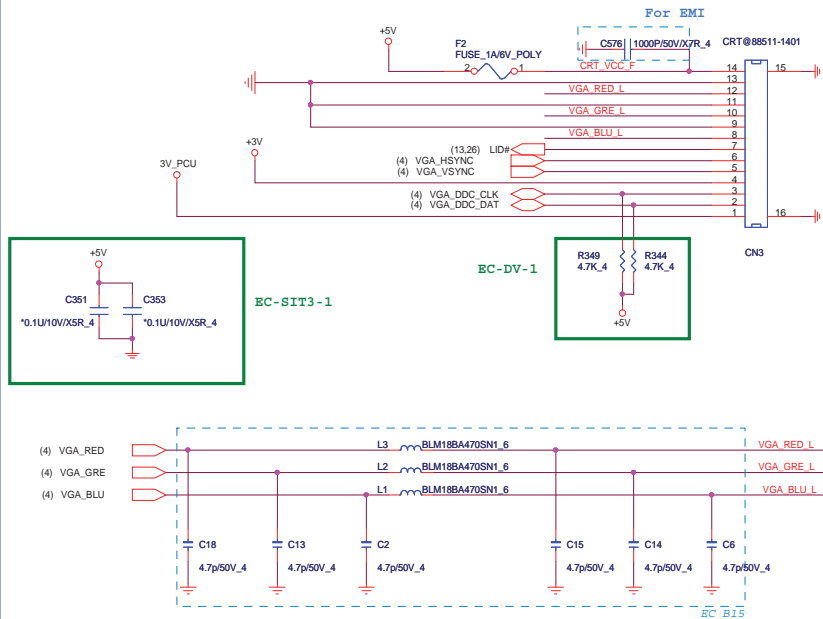


Quanta Computer Inc.

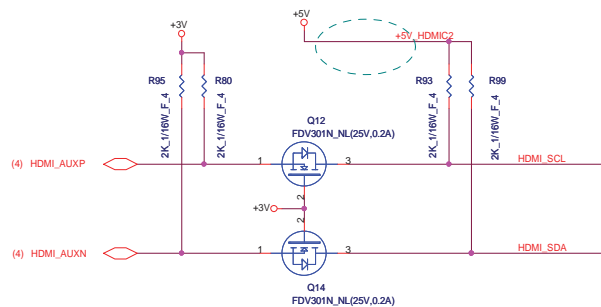
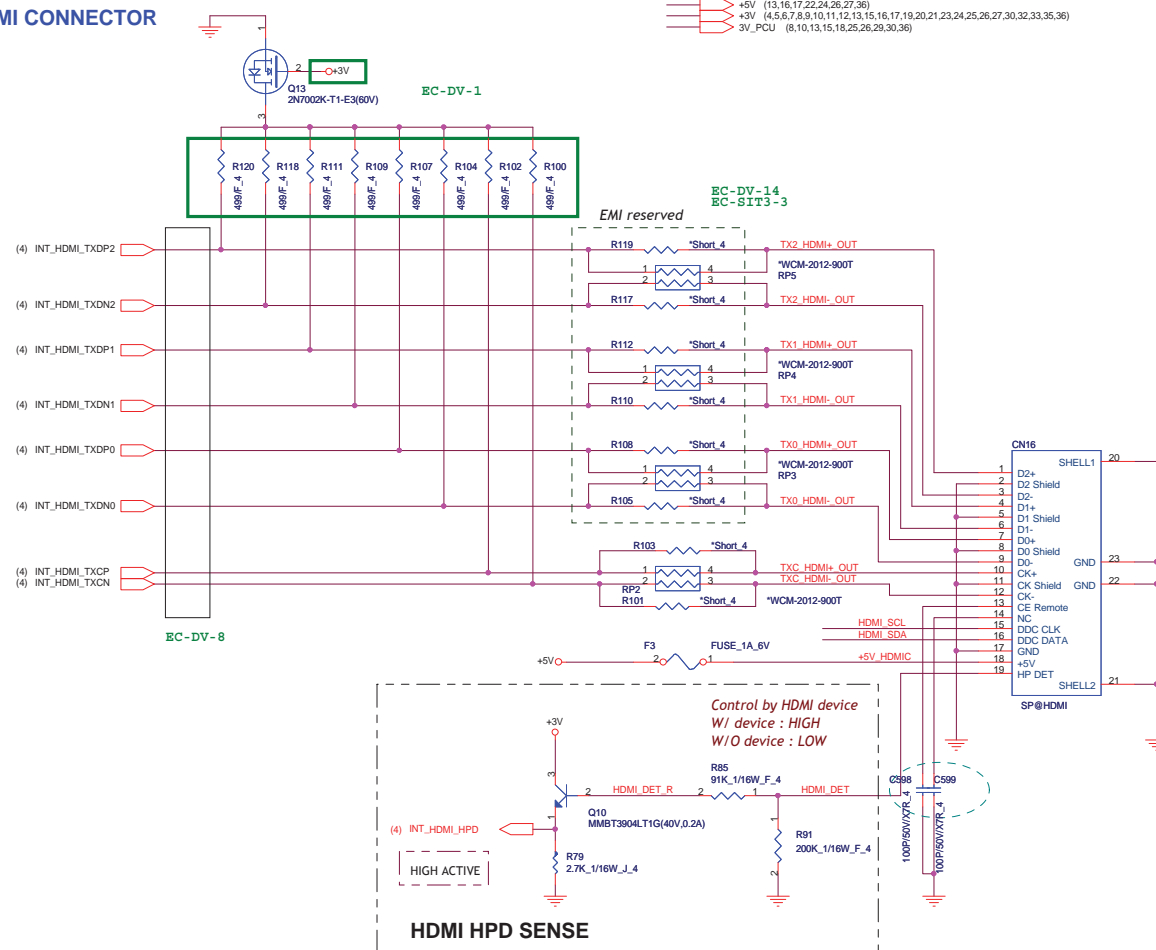
PROJECT : MK2.0

Size	Document Number	Rev
	LCD/CAMERA	1A
Date:	Friday, October 29, 2010	Sheet 13 of 47

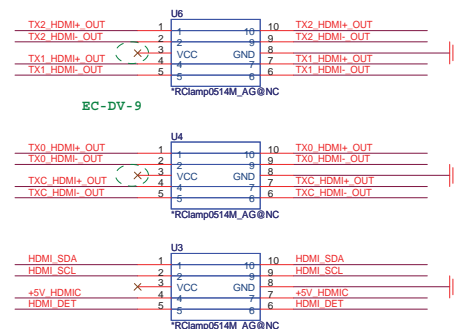
CRT FFC CONNECTOR



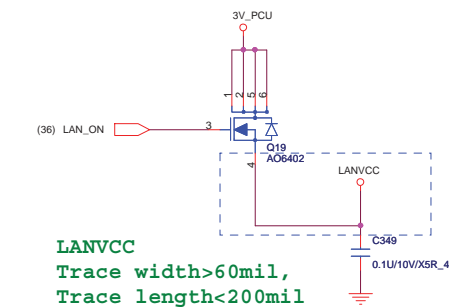
HDMI CONNECTOR



For ESD ---> Layout note: Place close to HDMI Conn

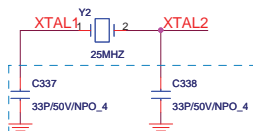


LANVCC

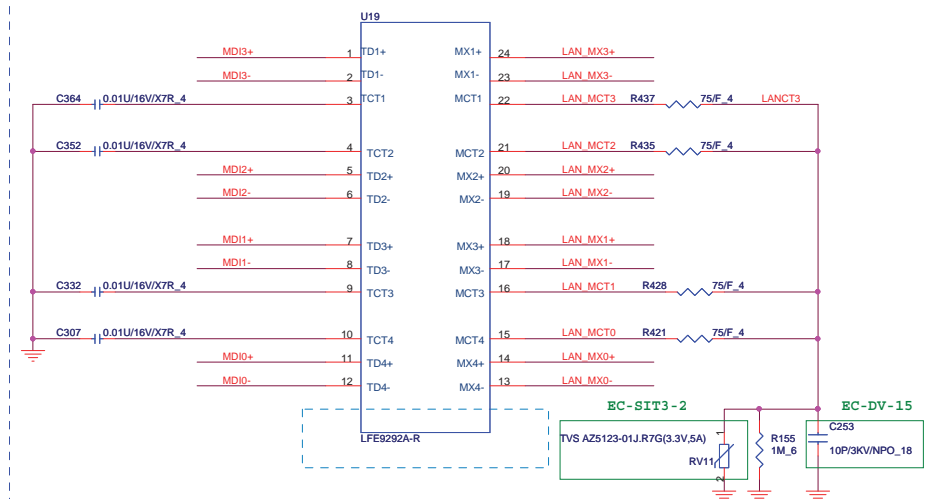


LANVCC

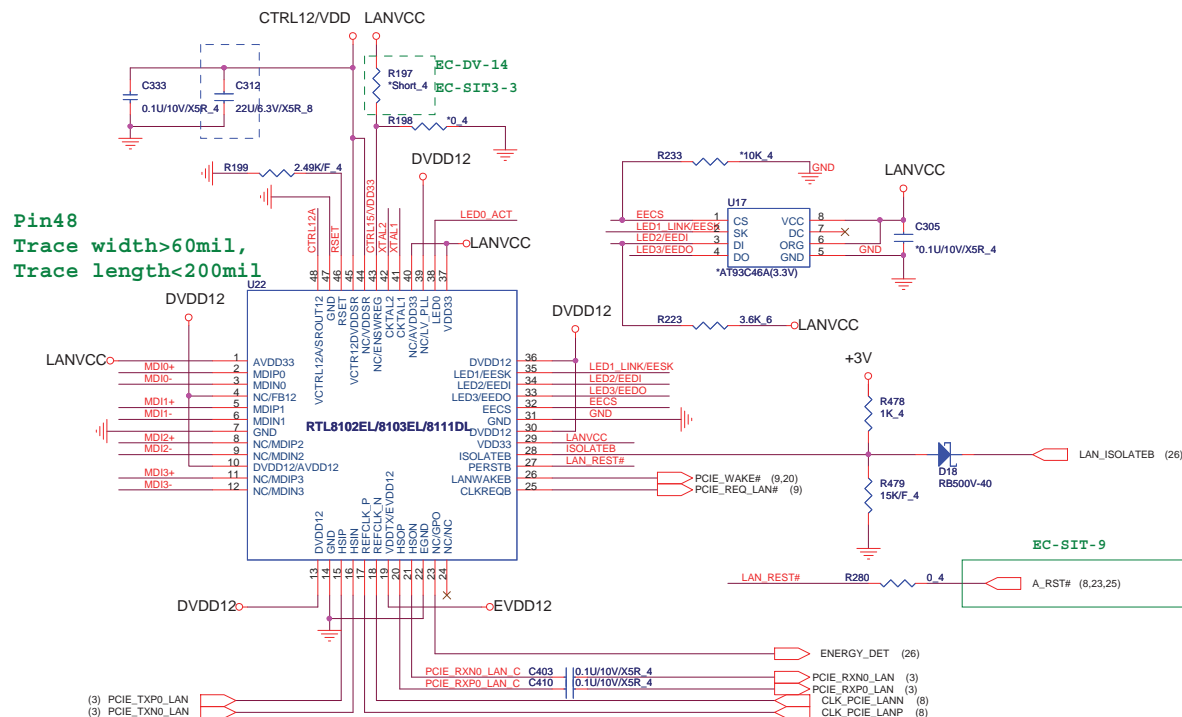
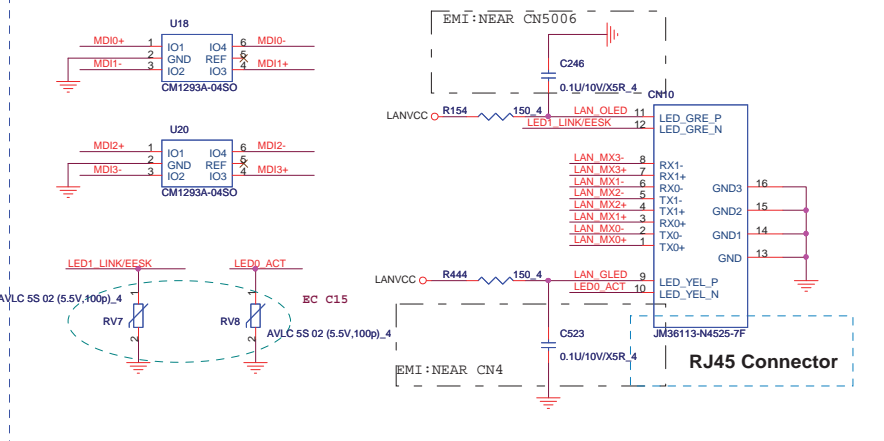
EC-DV-14
EC-SIT3-3



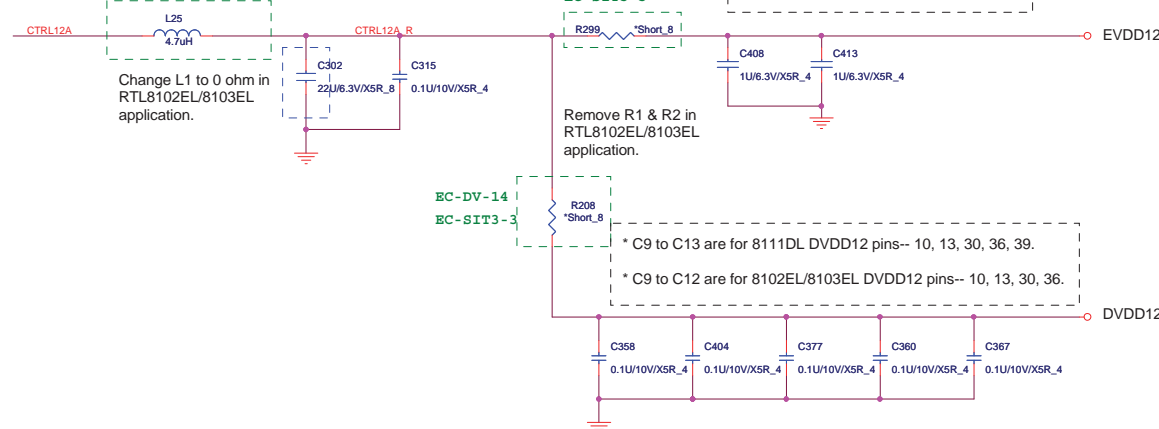
Transformer

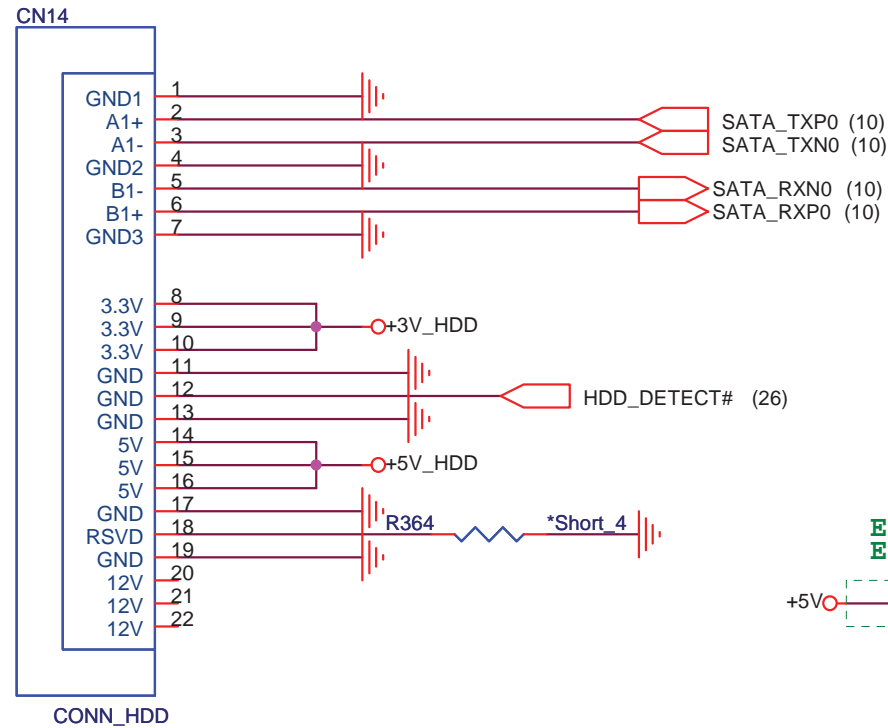


RJ45 Connector

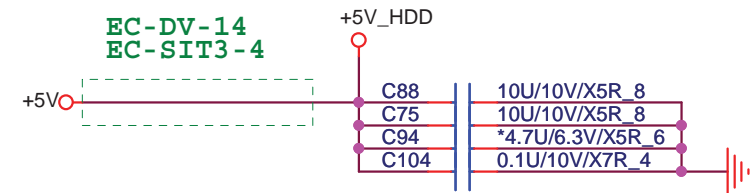


Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

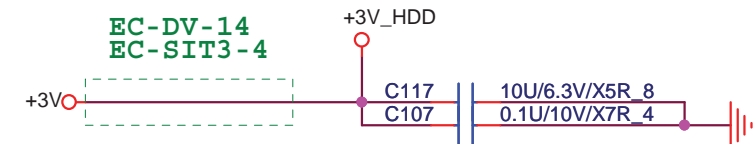




DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



Quanta Computer Inc.

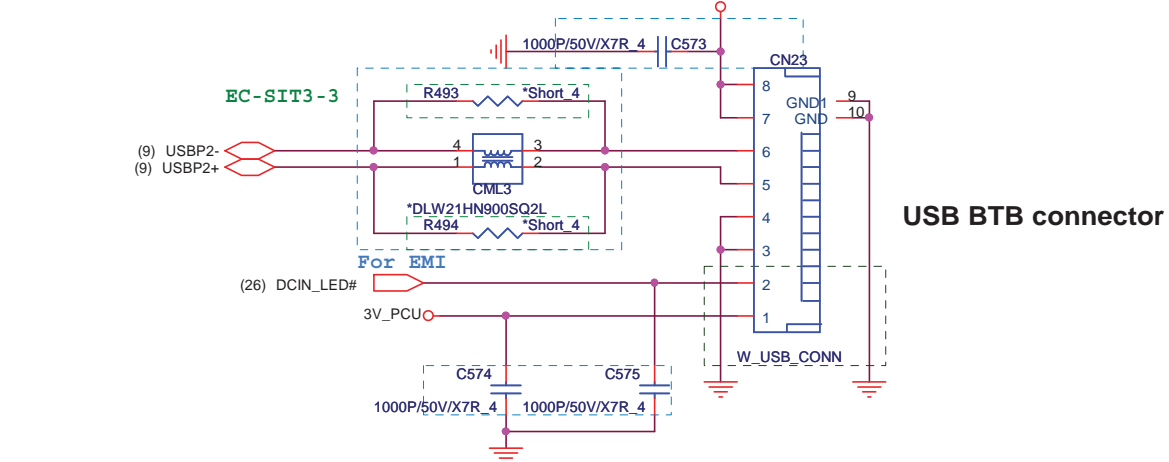
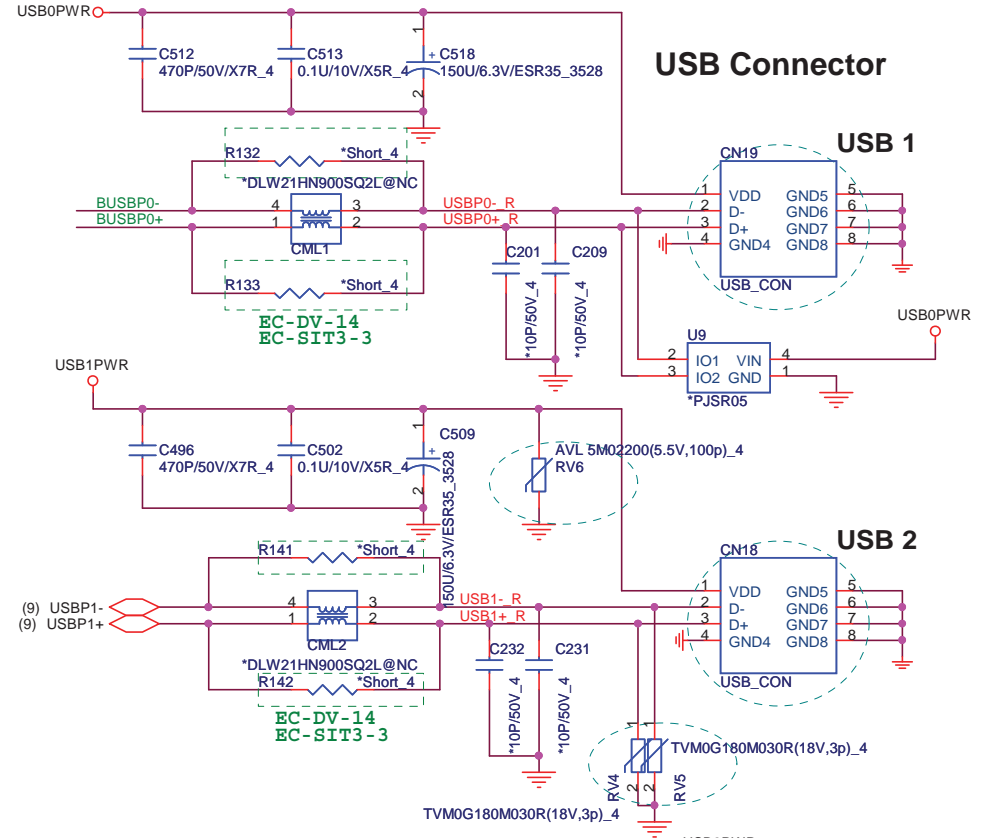
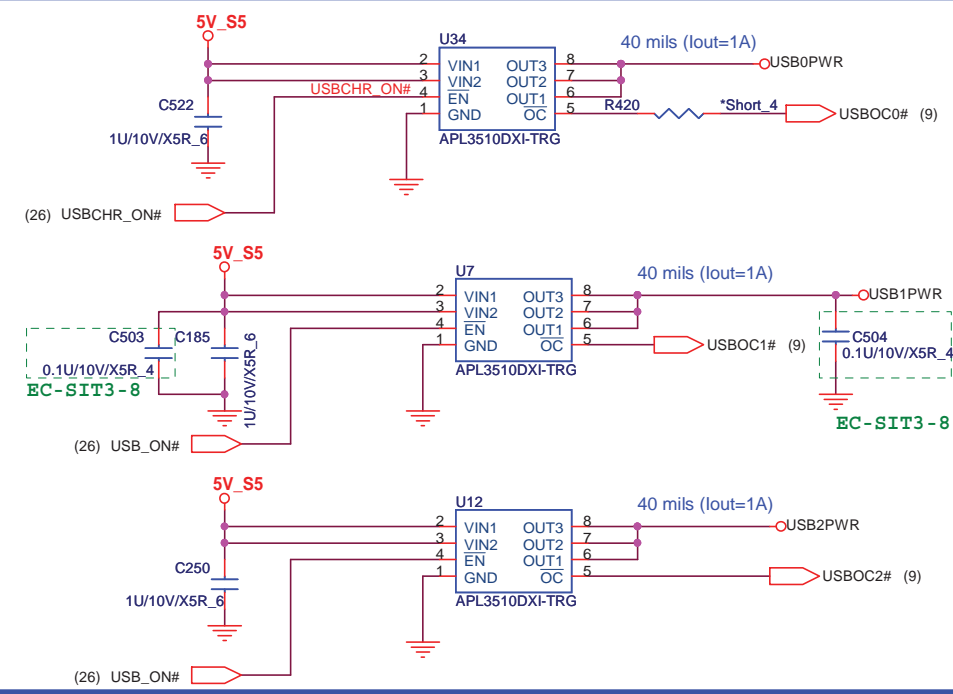
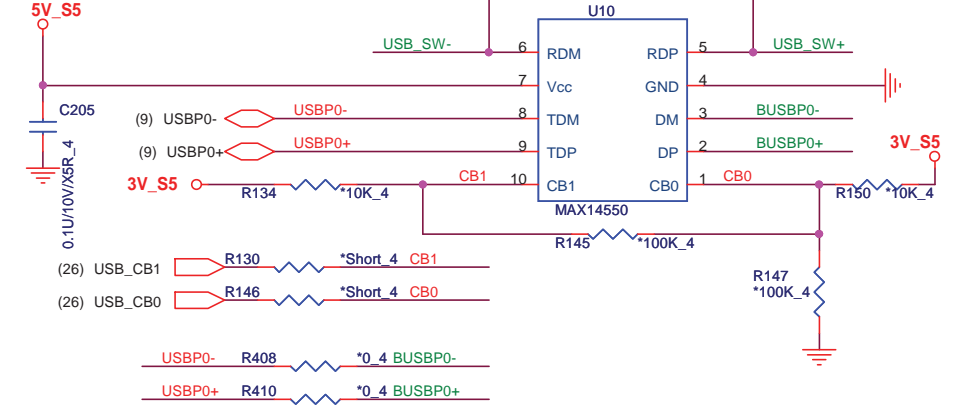
PROJECT : MK2.0

Size	Document Number	Rev
	SATA	1A
Date:	Friday, October 29, 2010	Sheet 17 of 47

USB SLEEP CHARGE (NEW)

CB0/CB1	Function	Int./Ext. R
0 0	S5 auto detect	Use Int. R
0 1	Blackberry(choice)	NC
1 0	iPod/iPhone(choice)	Use Ext. R
1 1	S0 auto detect	NC

Sleep charger notice



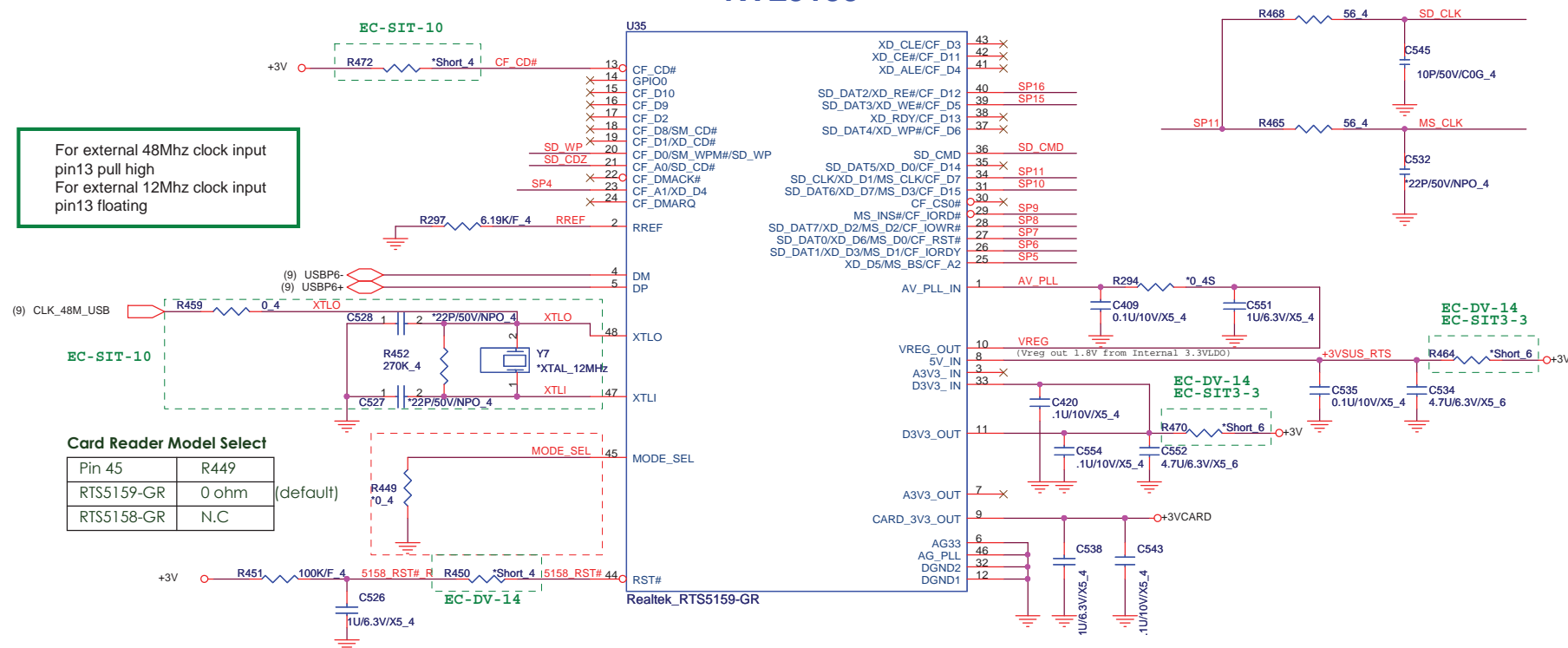
- 5V_S5 (36)
- 3V_S5 (8,9,10,11,12,20,23,25,26,36)
- 5V_SUS (13,25,32,34,35,36)
- 3V_PCU (8,10,13,14,15,25,26,29,30,36)

Quanta Computer Inc.

PROJECT : MK2.0

Size	Document Number	Rev
	USB x 3	1A
Date:	Friday, October 29, 2010	Sheet 18 of 47

RTL5159

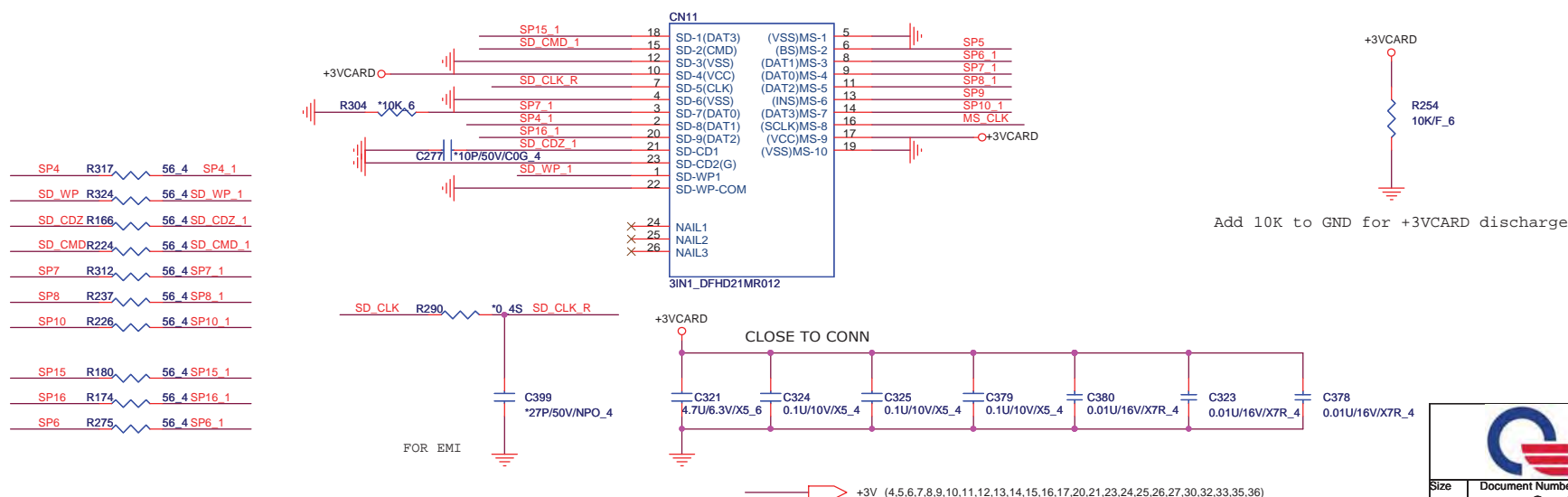


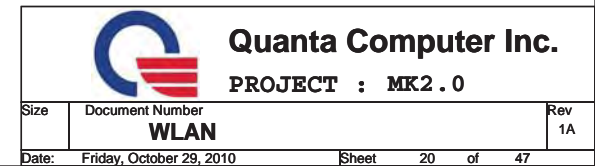
Note:

	SD/MMC	MS
SP0		
SP1		
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	
SP5		MS_BS
SP6		MS_D1
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9		MS_INS#
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	
SP13	SD_DAT4	
SP14		
SP15	SD_DAT3	
SP16	SD_DAT2	
SP17		
SP18		
SP19		

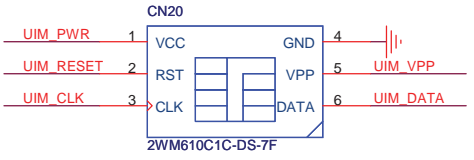
Card Reader Model Select	
Pin 45	R449
RTS5159-GR	0 ohm (default)
RTS5158-GR	N.C

3 IN 1 CARD READER

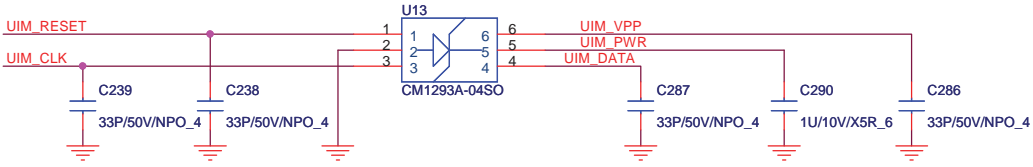




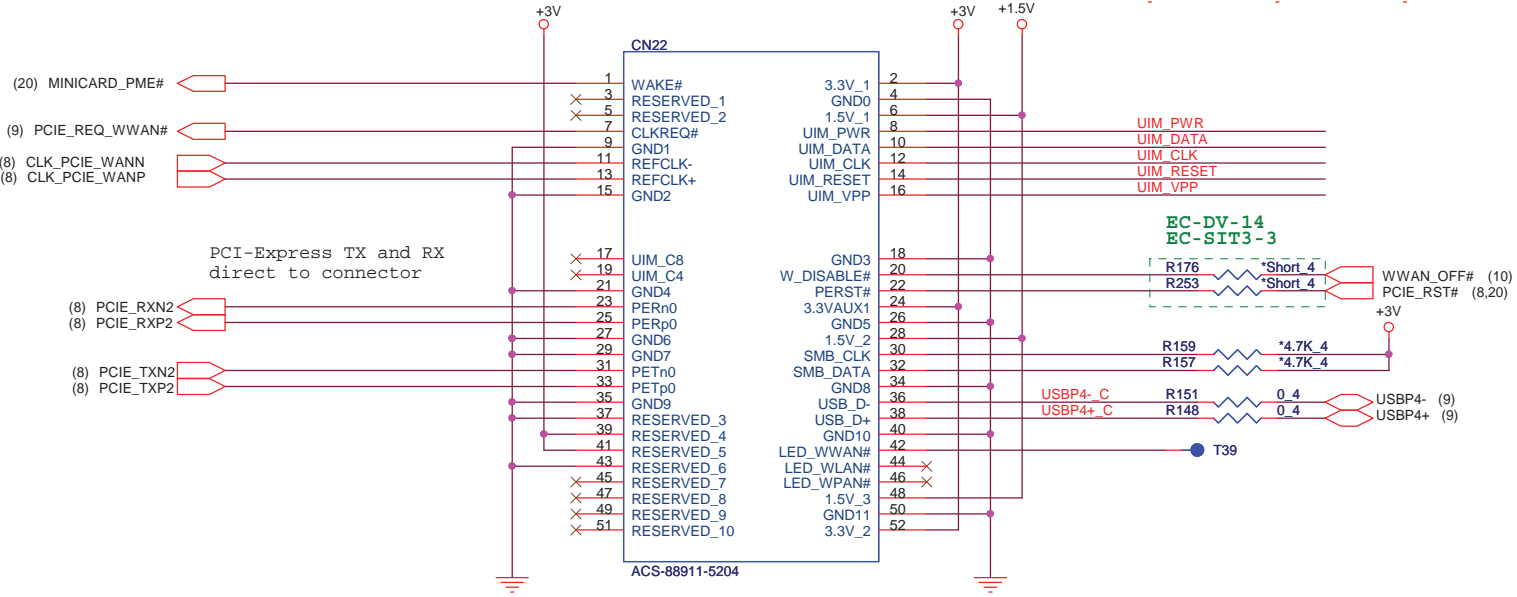
SIM Card CONN



Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routing as short as possible



MiniCard WWAN connector



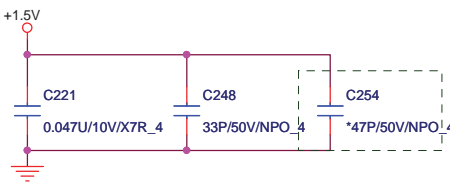
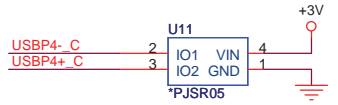
PCI-Express TX and RX direct to connector

EC-DV-14
EC-SIT3-3

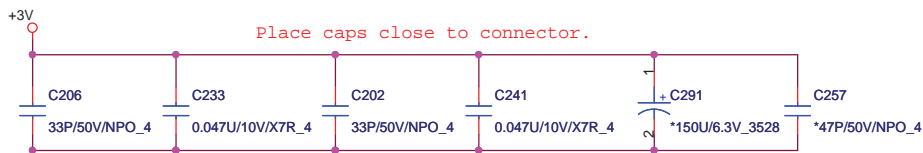
R176 *Short_4
R253 *Short_4

R159 *4.7K_4
R157 *4.7K_4

USBP4- C R151 0.4
USBP4+ C R148 0.4



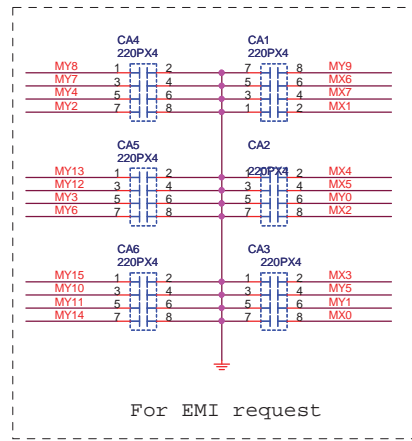
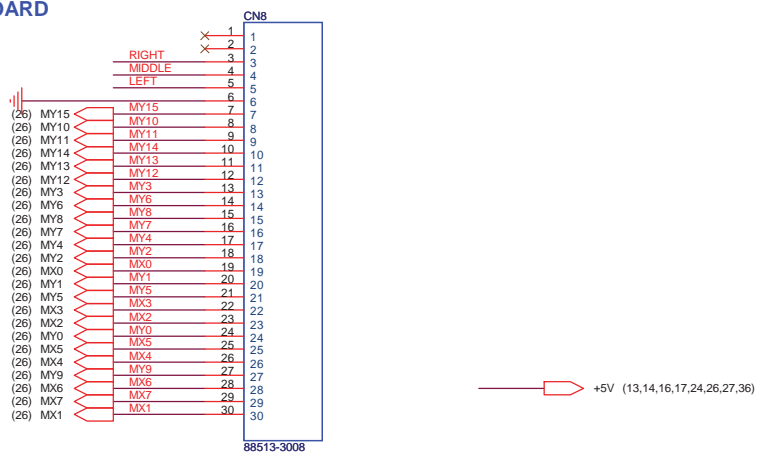
close to CN21



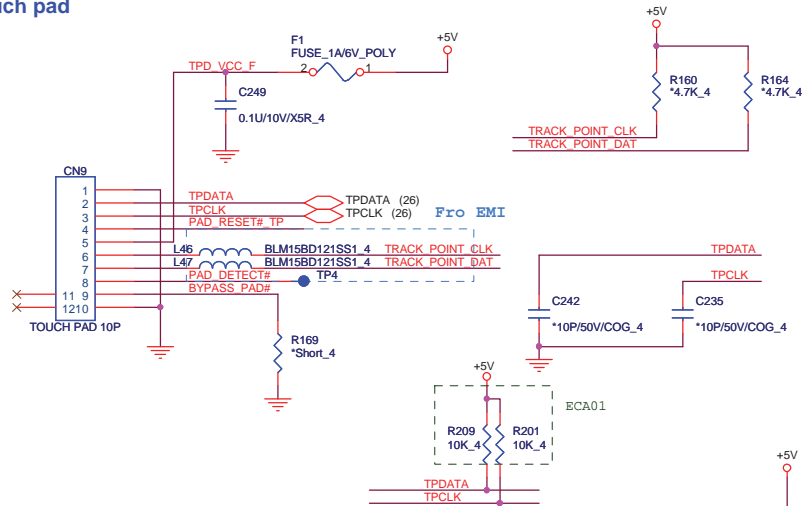
Place caps close to connector.

close to CN21

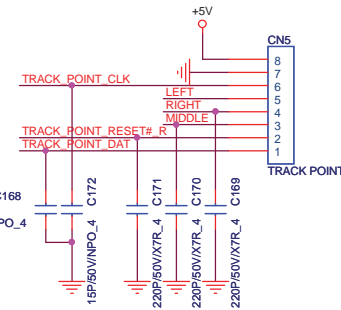
KEYBOARD



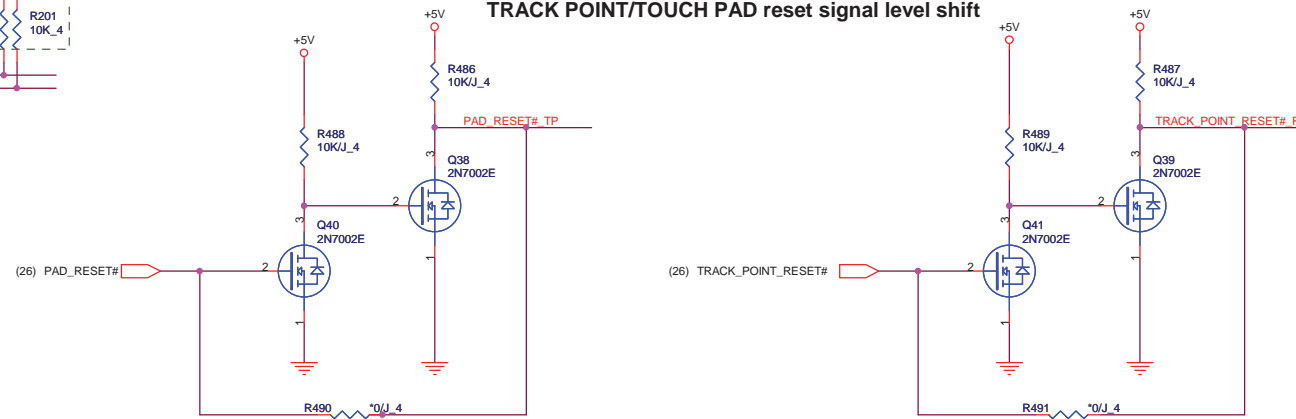
Touch pad



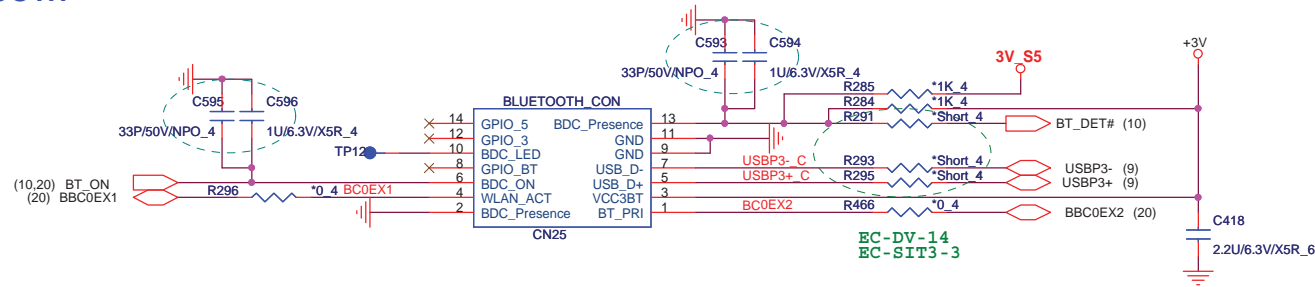
TRACK POINT



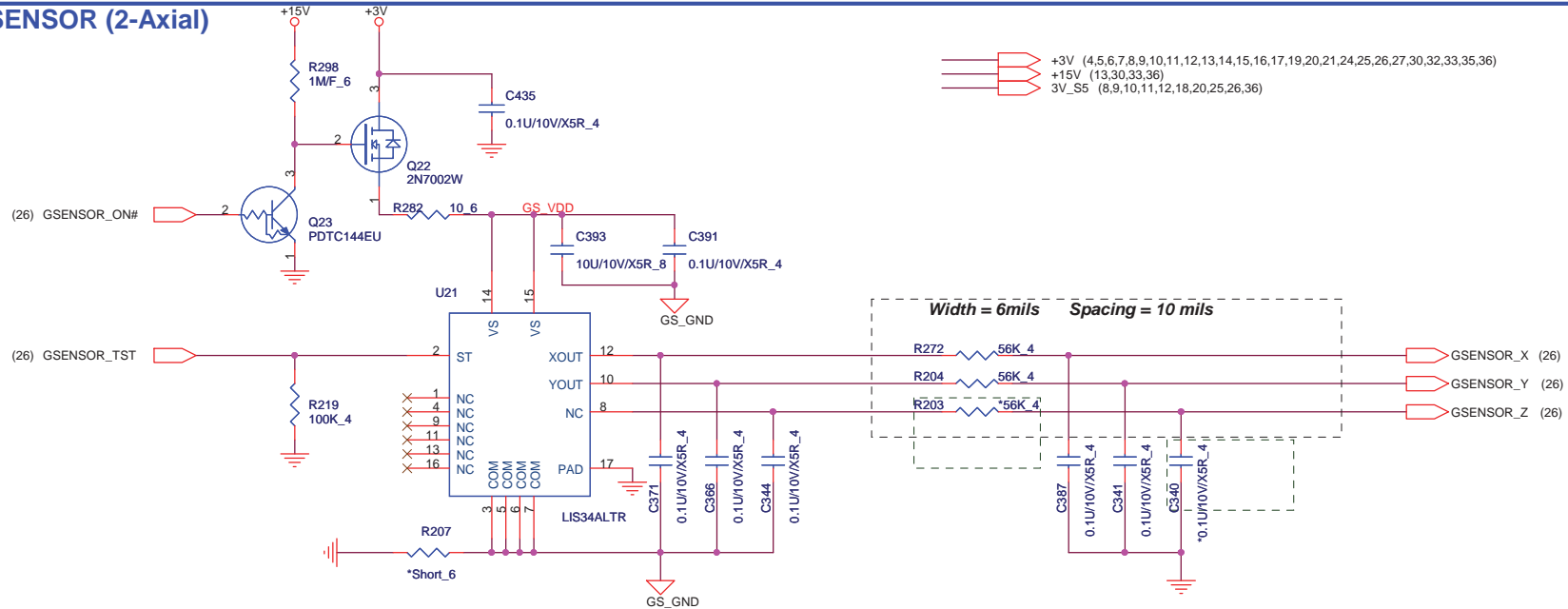
TRACK POINT/TOUCH PAD reset signal level shift



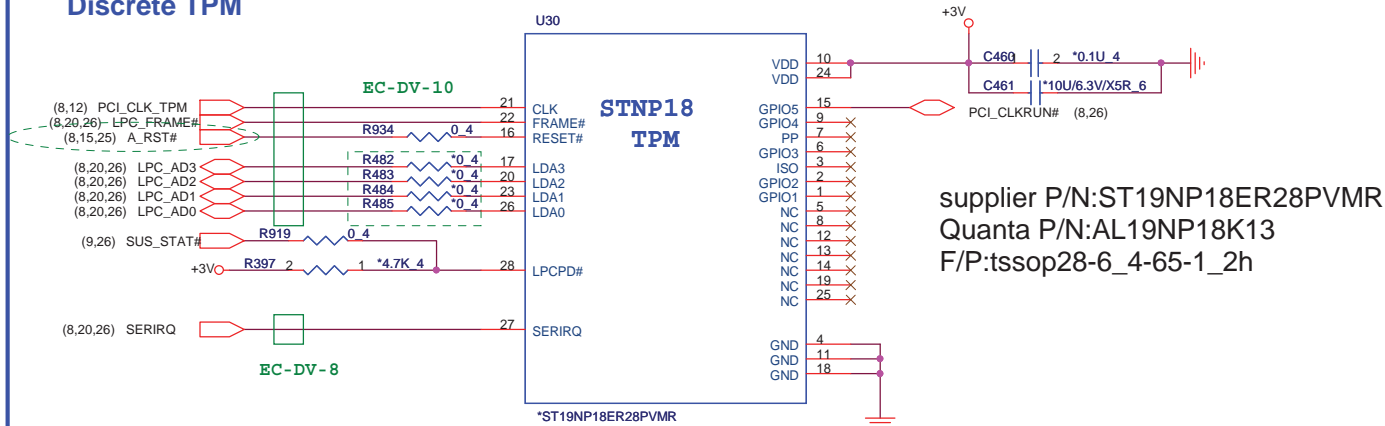
BLUETOOTH



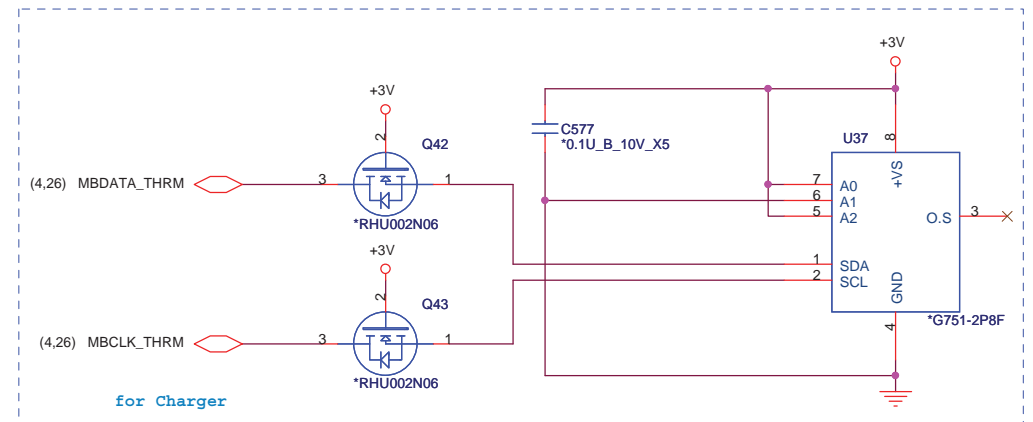
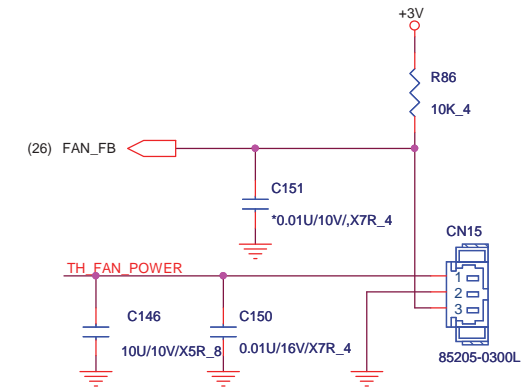
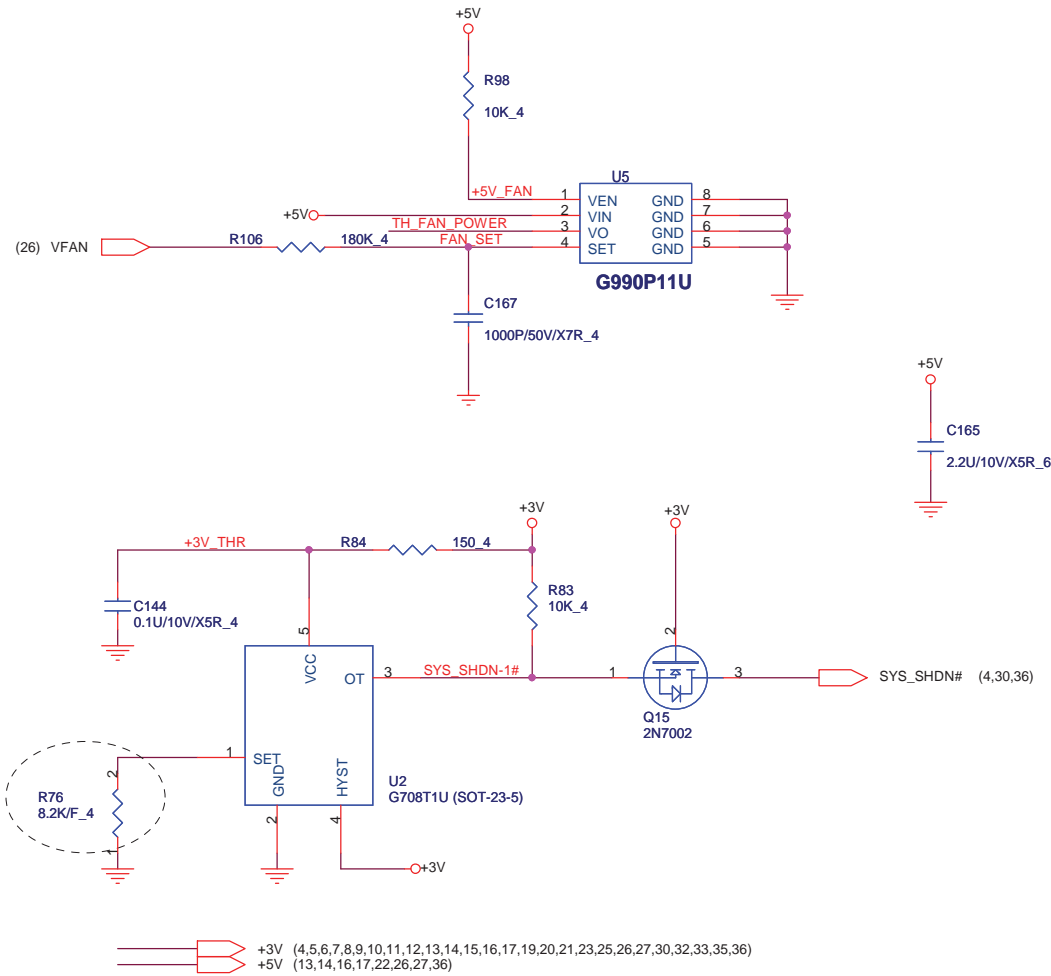
G-SENSOR (2-Axial)



Discrete TPM



FANPWR = 1.6*VSET



for Charger

ADDRESS: 9AH

ADDRESS							
1	0	0	1	A2	A1	A0	0
MSB				LSB			



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PROJECT : MK2.0

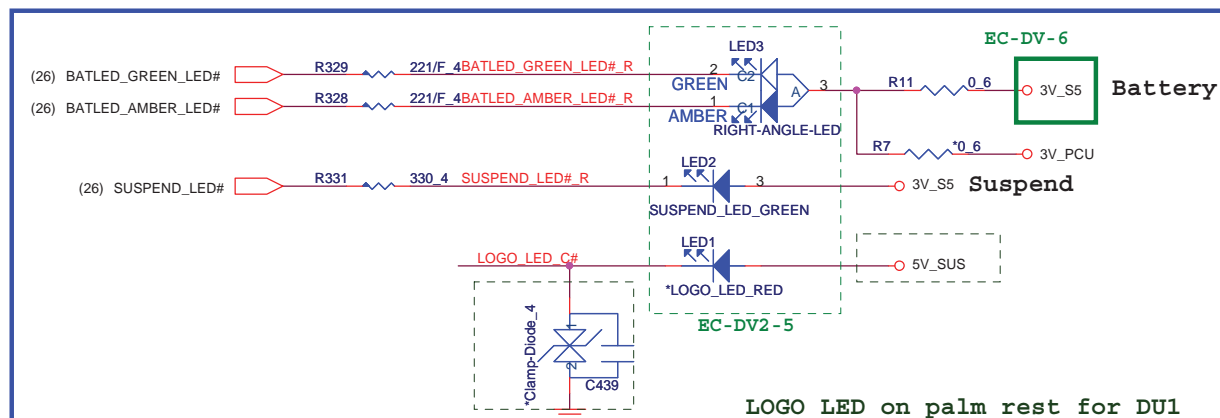
Size	Document Number	Rev
	FAN/Thermal	1A

Date: Friday, October 29, 2010

Sheet 24 of 47

The schematic diagram illustrates the I2C interface circuit for the G545B2P8U TSSOP package. The package pins are labeled: L1 (VCC), L2 (PROT), 6 (SCL), 5 (SDA), and 4 (GND). The external components include resistors R313 (4.7K₄), R322 (1K₄), R325 (*100K₄), and R318 (*100K₄), and a capacitor C436 (0.1u/10V/X5R₄). The power supply is +3V.

The I2C bus is connected to the HWPG and A_RST# signals. The HWPG signal is connected to pin 1 of D13 (CH500H-40) and pin 1 of D14 (CH500H-40). The A_RST# signal is connected to pin 2 of D13 and pin 2 of D14. The I2C bus is also connected to the G545B2P8U package. The SCL signal is connected to pin 6 (SCL) and pin 5 (SDA). The SDA signal is connected to pin 5 (SDA) and pin 4 (GND). The GND signal is connected to pin 4 (GND) and pin 5 (SDA). The VCC signal is connected to pin L1 (VCC) and pin L2 (PROT). The PROT signal is connected to pin L2 (PROT) and pin 6 (SCL). The SCL signal is connected to pin 6 (SCL) and pin 5 (SDA). The SDA signal is connected to pin 5 (SDA) and pin 4 (GND). The GND signal is connected to pin 4 (GND) and pin 5 (SDA).

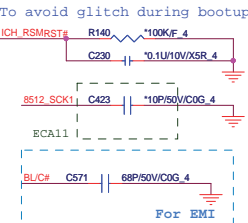
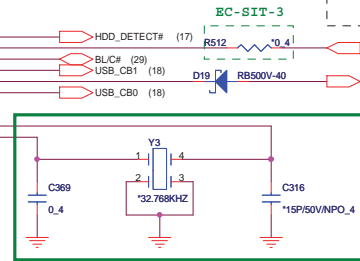
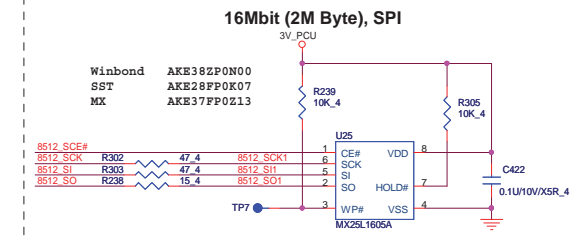
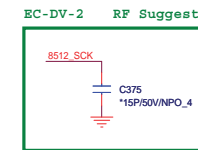
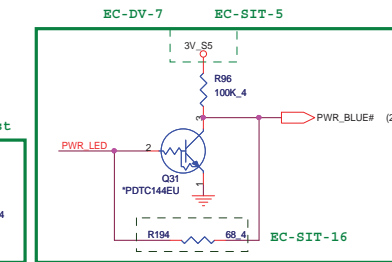
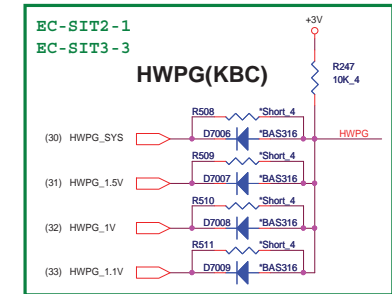
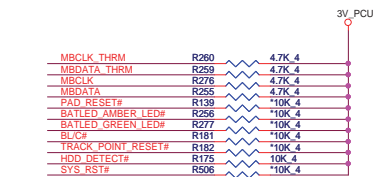


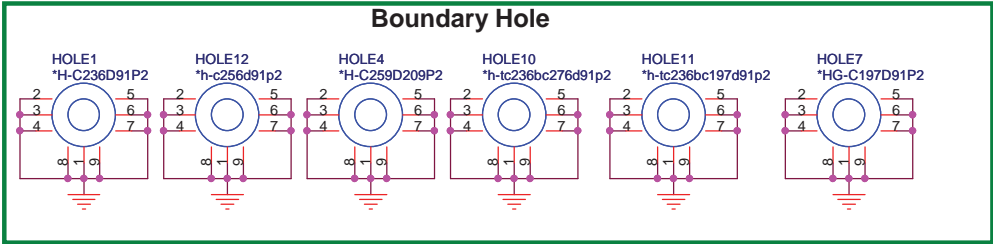
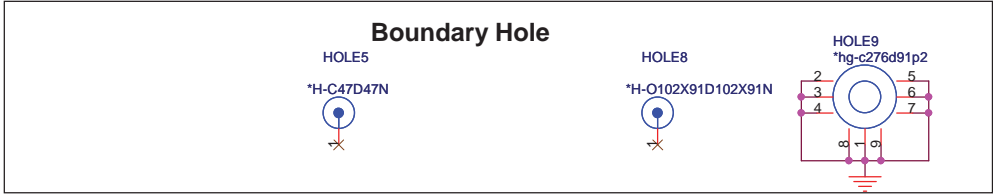
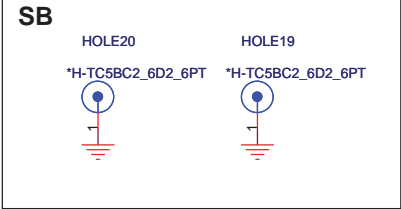
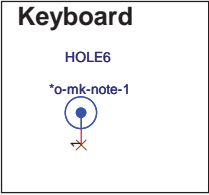
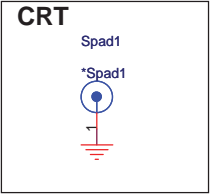
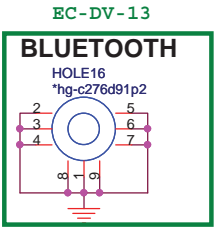
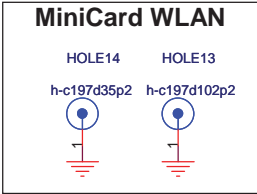
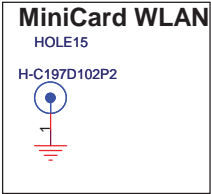
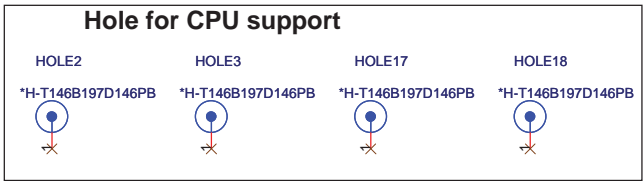
POWER BUTTON

The schematic diagram illustrates the power button circuit. It features a power switch (CN2) connected to a network of resistors (R4, R6, R10) and capacitors (C562, C563). The circuit is protected by EMI components (Fro EMI) and includes a 3V_S5 supply. A 3V_PCU supply is connected to a 10K resistor (R5) and a diode (C7) to ground. The circuit is labeled with various components and their values.

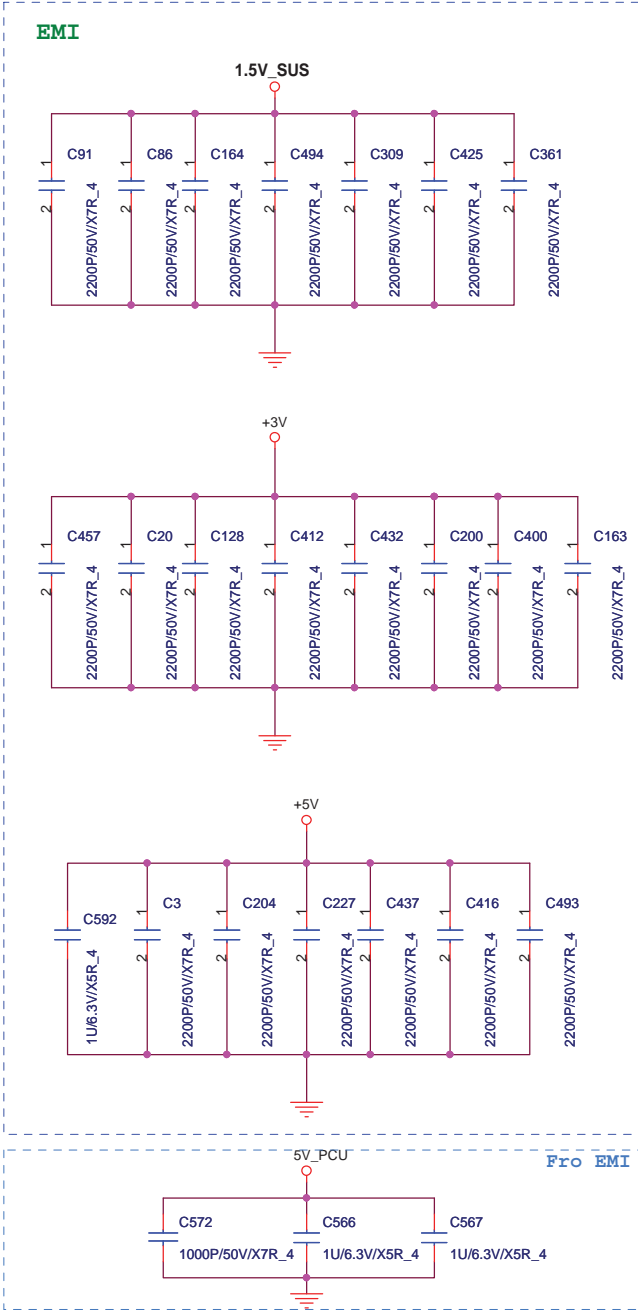
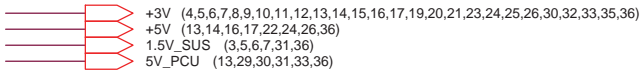
Key components and labels include:

- POWER switch**: The physical button switch.
- CN2**: Connector for the power switch.
- EC-DV-14**: A component, possibly a diode or capacitor, connected to the switch.
- EC-SIT-4**: A component, possibly a diode or capacitor, connected to the switch.
- 3V_S5**: A 3V supply source.
- 3V_PCU**: A 3V supply source.
- R4, R6, R10**: Resistors with values of 0.6.
- C562, C563**: Capacitors with values of 2200P/50V/X7R_4.
- Fro EMI**: EMI protection components.
- R5**: A 10K resistor.
- C7**: A capacitor with a value of 15P/50V/NPO_4.
- 0.1U/10V/X5R_4**: A capacitor value.
- (26) NBSWON#** and **(26) PWR_BLUE#**: Signal pins.



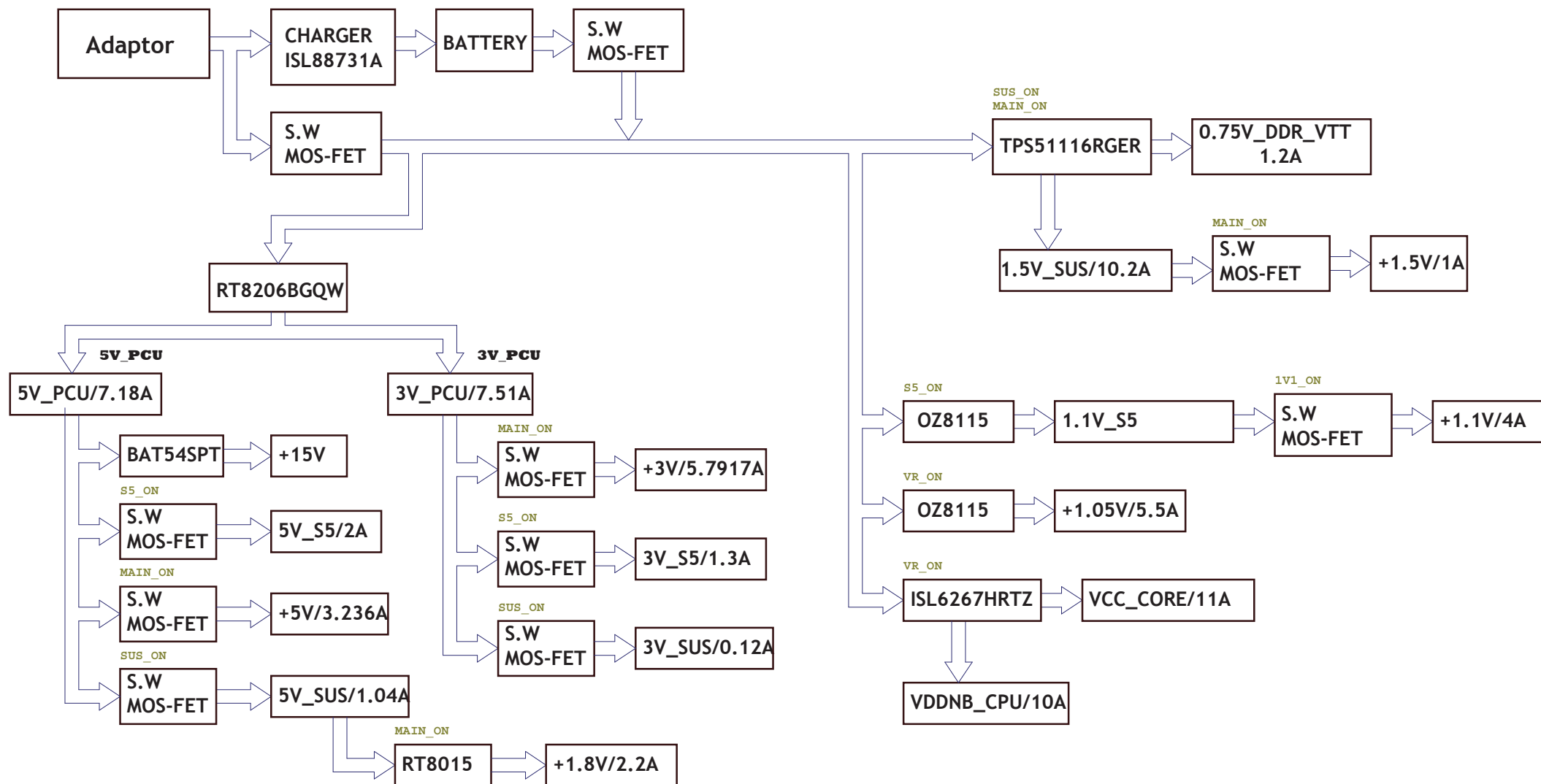


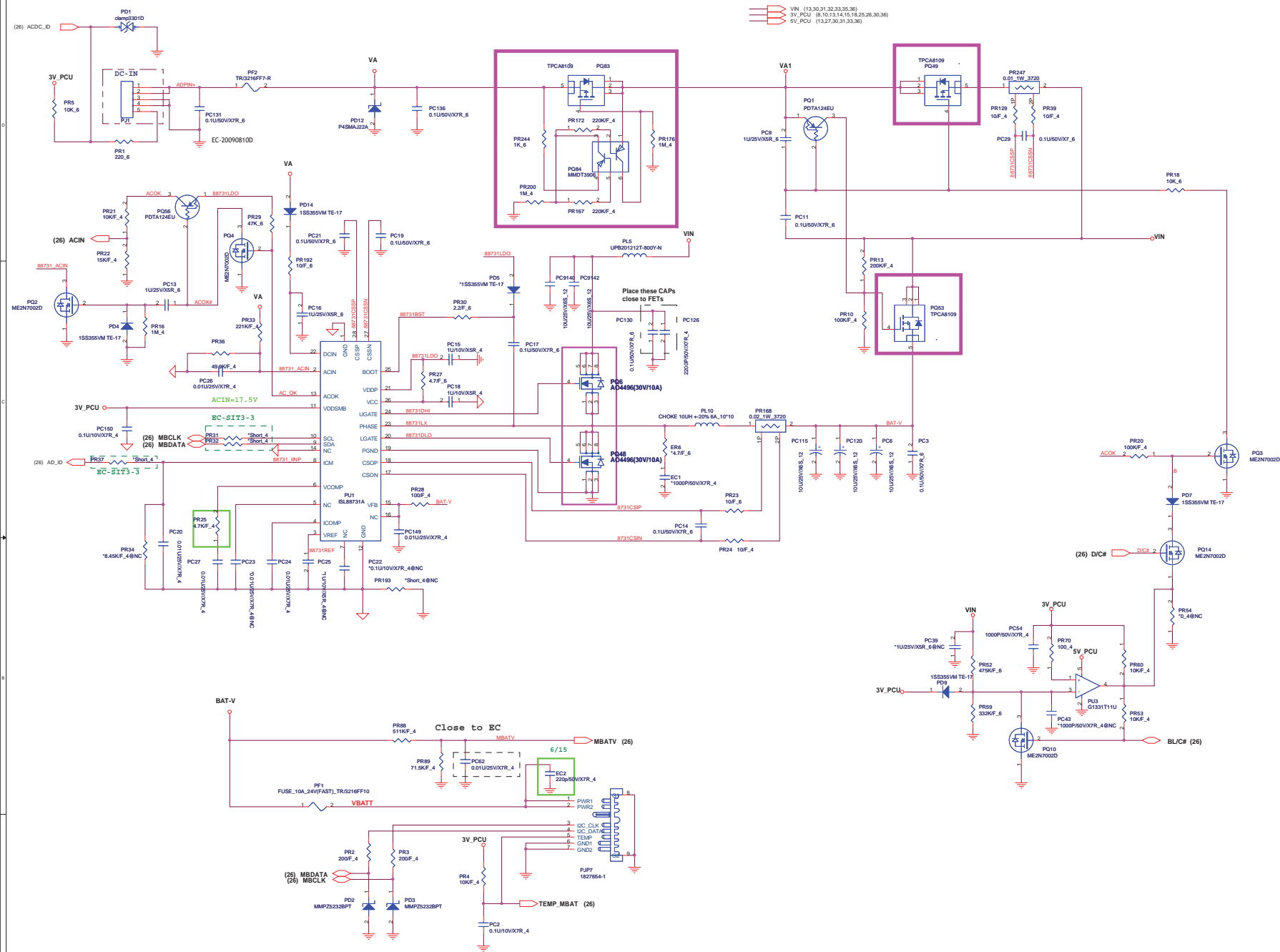
EC-DV-13

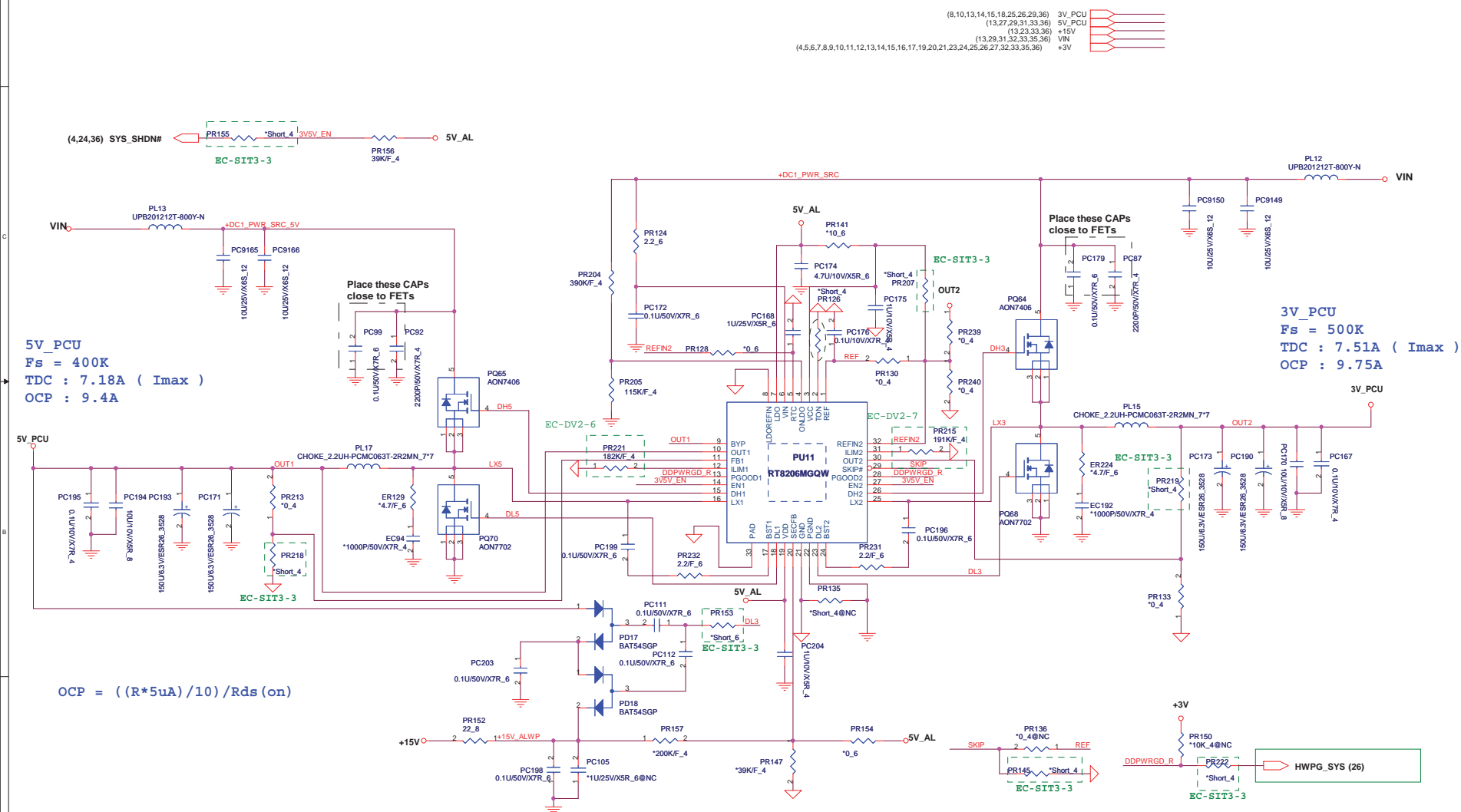


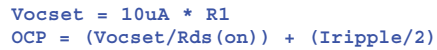
Brazos SYSTEM POWER BLOCK DIAGRAM

28







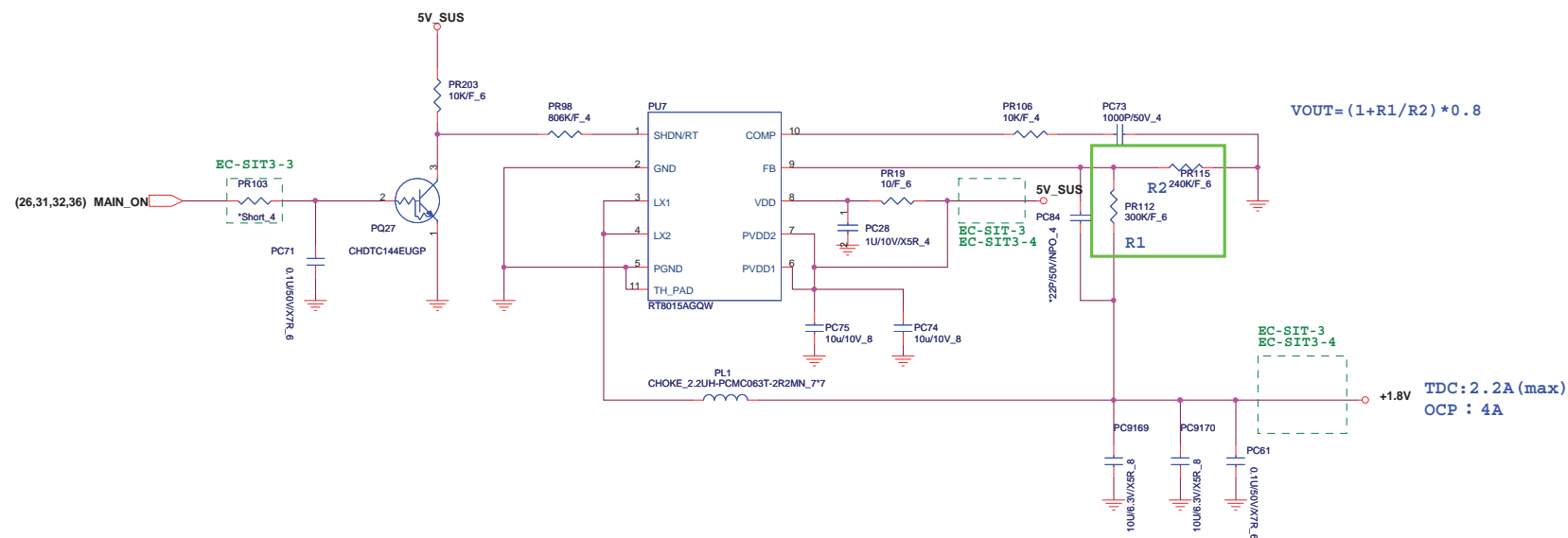




VIN=20V, FSW (KHZ)=236K

VIN=9V, FSW (KHZ) =219K

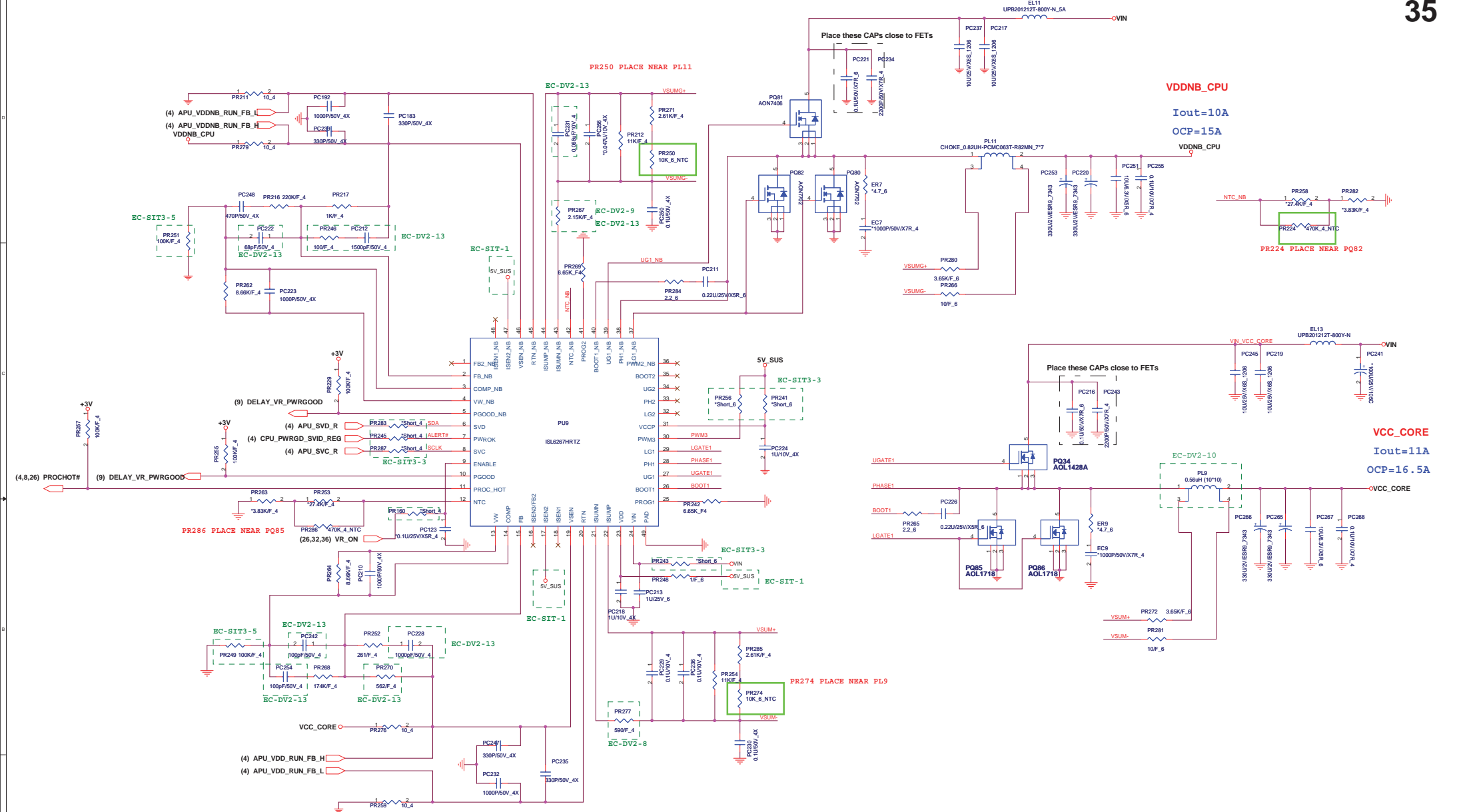
$$I_{out}=6A$$
$$O.C.P.=7.8A$$
$$V_{set} = 2.75 * (R_2 / (R_2 + R_3))$$
$$\text{Freq.} = (V_o * (V_i - V_o)) / (4.4u * V_i)$$
$$I_{out} = 4A$$



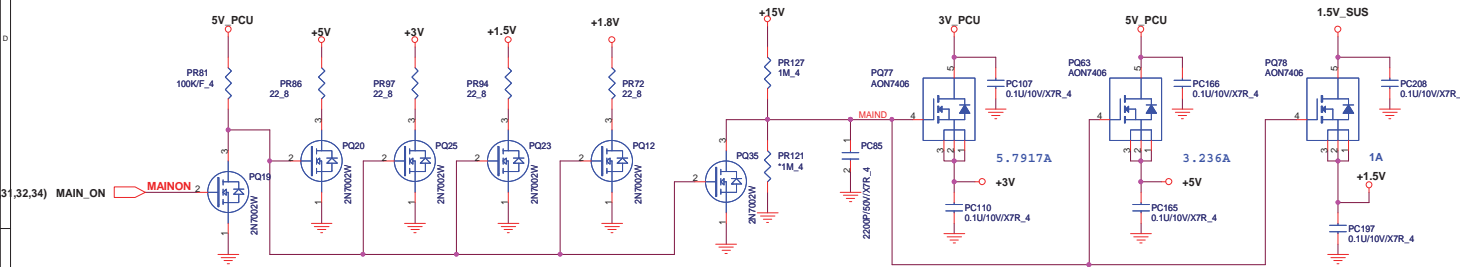
Quanta Computer Inc.

PROJECT : MK2.0

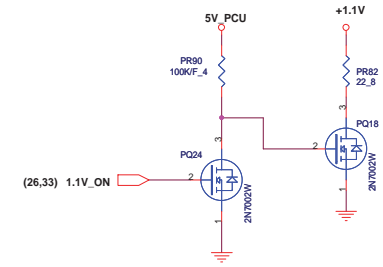
Size	Document Number	Rev
	+1.8V (RT8015AGQW)	1A
Date:	Friday, October 29, 2010	Sheet 34 of 47



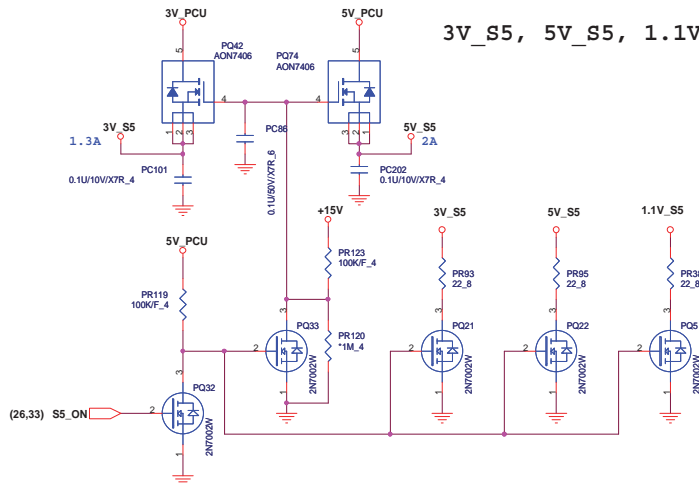
+3V, +5V, +1.8V, +1.5V



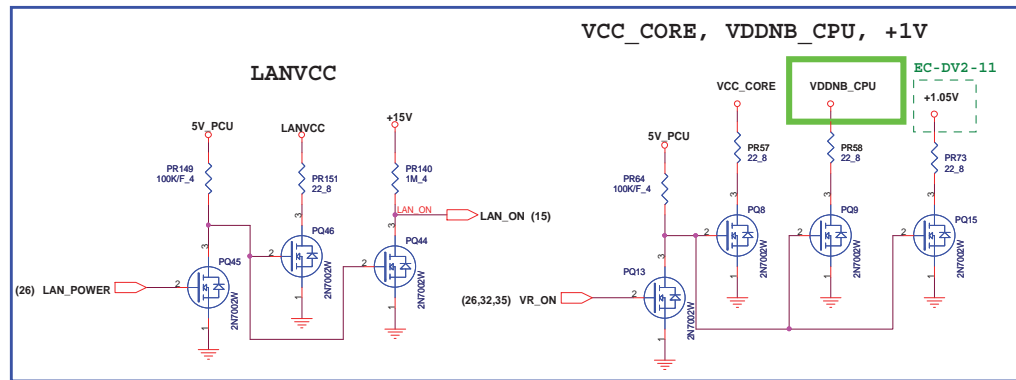
+1.1V



3V_S5, 5V_S5, 1.1V_S5

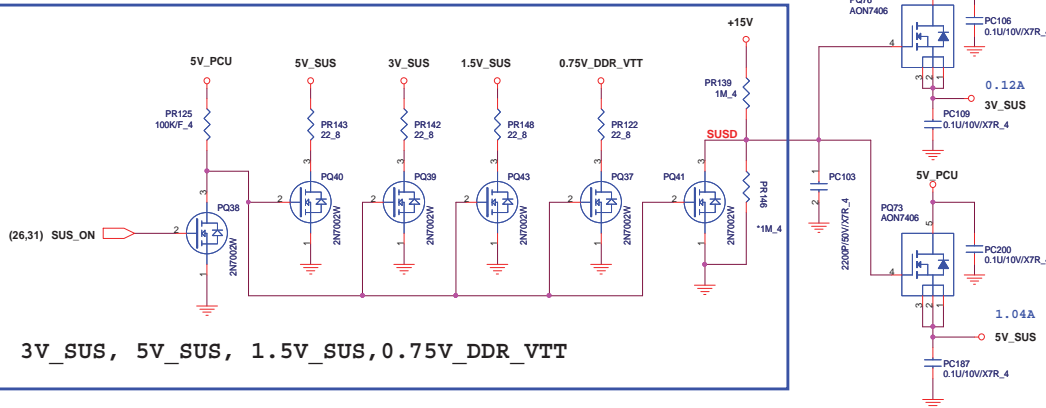


LANVCC

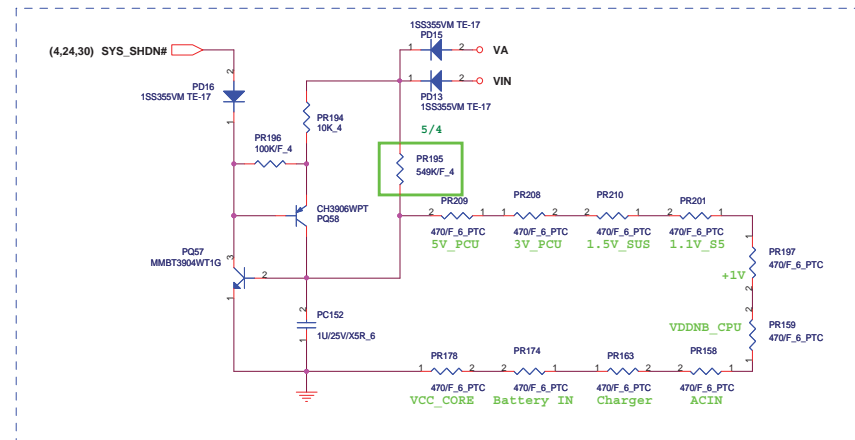


VCC_CORE, VDDNB_CPU, +1V

3V_SUS, 5V_SUS, 1.5V_SUS, 0.75V_DDR_VTT

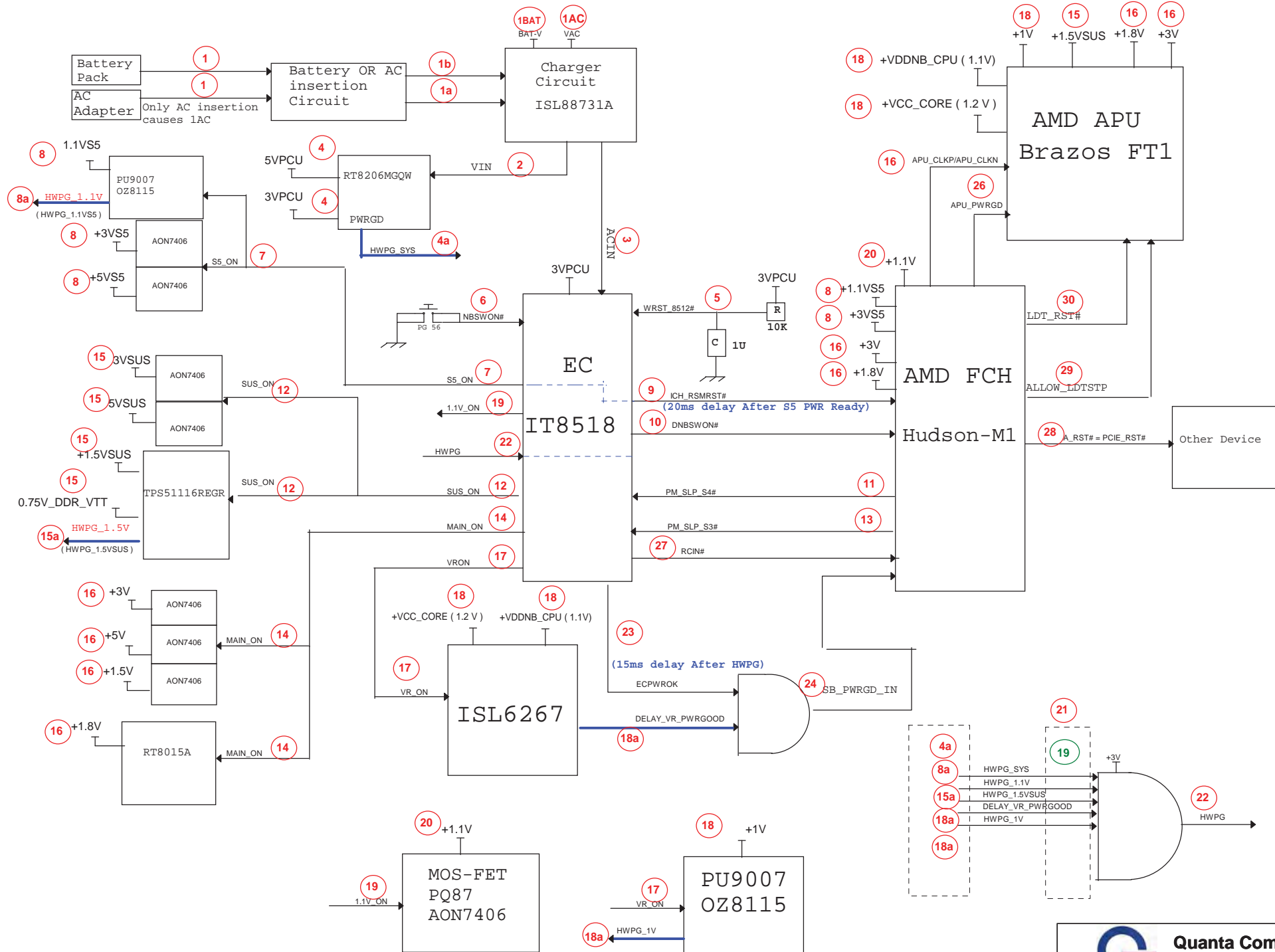


(4,24,30) SYS_SHDN#



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PROJECT : MK2.0



[illegible]

Revision History

39

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
A1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP


CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

EC #	Page	Date	Part Affected	Description
EC-DV-01 (AMD Suggest)	11	10/08/01	C1094	Change value from 0.1U to 1U
	11	10/08/01	L60	Add a Inductor and connect to VDDPL_1.1V
	11	10/08/01	C1073	Change value from 4.7U to 2.2U
	11	10/08/01		PCH NET"XDDXL_33_S" change power rail from 3V_S5 to +3V
	4	10/08/01	R728	Because Prochot# has been pull up +3V, delete one pull up resistor. Delete R728.
	8	10/08/01	C1042, C1045, C1043, C1044	Change value from 18P to 22P.
	10	10/08/01	U44	Change SPI ROM input and output with PCH.
	4	10/08/01	R92	"LTDPO_APD"add pull down resistor
	4	10/08/01	R739,R740	Delete R739, R740
	14	10/08/01	R344,R349	"VGA_DAC_SDA and VGA_DAC_SCL" add pull up 4.7k resistor from +3V to +5V power rail.
	14	10/08/01	R100,R102,R104,R107,R109,R111,R118,R120	Change resistor value to 499 ohm
	14	10/08/01	Q13	Change Q13 power rail from +3X to +5V
	03	10/08/01	C871, C19	Add C871 and C19
	06	10/08/01	R123,R163	Change value from 10k to 1K
	11	10/08/01		Change "VDDIO_AZ" from +1.5V_SUS to +3V
	9	10/08/01	R324	Change value from 4.7K to 10K
	9	10/08/01	R324	USBOC1# and USBOC2# change pull up voltage from 3V_SUS to 3V_S5
EC-DV-02	8 9 10 26	10/08/02	C376,C381 C382, C370 C375	Add RF tesm suggest
EC-DV-03	9	10/08/02	RP12	Change footprint type for layout
EC-DV-04	26	10/08/02	U15	Change EC from IT8502E to IT8518
EC-DV-05	26	10/08/02	R192, R195	To prevent EC leakage issue
EC-DV-06	25	10/08/02		Change battery LED power rail from 3V_PCU to 3V_S5
EC-DV-07	26	10/08/02	R96,Q31	Fro EC suggest, change power LED control singnal from low active to high active.
EC-DV-08	14 23	10/08/02		Celete duplicate net.
EC-DV-09	14	10/08/02		Delete GND net of pin3 from U4 and U6

[illegible]

EC #	Page	Date	Part Affected	Description
EC-DV2-1	13	10/08/24	CN27,R342,R348	Because LVDS CONN still combine, delete USB component.
EC-DV2-2	9	10/08/24	R937,R938,R849,R851	EPROM setteing from SPI to LPC ROM.
EC-DV2-3	32	10/08/24	PR9153,PR9169	AMD Suggest it to meet power sequence.
EC-DV2-4	3,8	10/08/24	C109,C110	AMD Suggest that use APU PCIe interface to link LAN to enhance its performance.
EC-DV2-5	25	10/08/24	LED1,LED2,LED3	For ID design. Delete LED1 ,add LED2 and LED3
EC-DV2-6	30	10/08/24	PR221	For 5V_PCU OCP
EC-DV2-7	30	10/08/24	PR215	For 3V_PCU OCP
EC-DV2-8	35	10/08/24	PR277	For VDDNB_CPU OCP
EC-DV2-9	35	10/08/24	PR267	For VCC_CORE OCP
EC-DV2-10	35	10/08/24	PL9	For CPU Ripple voltage
EC-DV2-11	32	10/08/24	PR9167	For AMD request change +1V to +1.05V
EC-DV2-12	31	10/08/24	PC169	For 1.5V_SUS output ripple voltage
EC-DV2-13	35	10/08/24	PC231,PC212,PR246,PC222,PC242, PC228,PC254,PR270,PR267	Chip vendor suggest.
EC-DV2-14	26	10/08/24	D7006,D7007,D7008,D7009,R508,R509,R510,R511	Mount Diode for easy debug



Quanta Computer Inc.

PROJECT : MK2.0

Size	Document Number	Rev
	EC list for DV2	1A
Date: Friday, October 25, 2010	Sheet 42 of 47	

EC #	Page	Date	Part Affected	Description
EC-SIT-1	35	10/09/17	PU9	Chip vendor(Intersil) suggest that some power chip pin change from +5V to 5V_SUS to prevent 5V leakage current.
EC-SIT-2	31~34	10/09/17	PJP2,PJP6,PJP12,PJP13,PJP14,PJP15, PJP16,PJP17,PJP18	Power jump PCB footprint change from open type to short type
EC-SIT-3	26	10/09/17	R512	For S3/S4/S5 leaksge issue from 20mA to 5mA. This pin is re-define from output to input. But EC don't use this pin. Resever it.
EC-SIT-4	25	10/09/17	CN2 pin4	Power LED plan change from 3VPCU to 3V_S5 to prevent LED flight one tie issue during plug adapter. Fix ECR72256 from Vendor(ITE) suggestion
EC-SIT-5	26	10/09/17	Q31, R194	Power LED enable lever from high active to low active. Delete Q31, add R194. Fix ECR72256 from EC team member request
EC-SIT-6	25 13	10/09/17	Q24,Q21,Q25,R311,R301,R288,R314 C568	Because MK2B don't support Logo LED function, delete them. Delete Q24,Q21,Q25,R311,R301,R288,R314,C568
EC-SIT-7	13	10/09/17	R12	Reserve R12(short pad) to prevent LCD short current verication.
EC-SIT-8	6 7	10/09/17	C7274, C7275	Change DDR DIMM Module VREF_CA and VREF_DQ reference power.
EC-SIT-9	15	10/09/17		Because LAN interface cahnge FCH to APU, change its reset signal from PCIE_RST# to A_RST#.
EC-SIT-10	19	10/09/17	Y7, C257, C258,R472,R459	Cardreader clock input from 12MHZ crystal to FCH internal clock.
EC-SIT-11	5	10/09/17	C927, R9796,C934	Delete C927,C934 for layout. Add R796 for AMD suggest.
EC-SIT-12	8	10/09/17	C1111	Reserve a capacitor for RF team request.
EC-SIT-13	11	10/09/17	L48,L50,L52	AMD suggest. Change its current sustain from 1.5A to 5A.
EC-SIT-14	10	10/09/17	R881,R884,R885,R877,R878,C1058	Because BIOS and EC use the same ROM, delete them from BOM.
EC-SIT-15	8	10/09/27	C1043,C1044	Crystal vendor suggest(TXC and Hosonic)that chage fromm 22P to 10P to get good sin=gnal
EC-SIT-16	26	10/10/05	R194	Change value from 0 ohm to 68 ohm to meet ITE8518 current limit issue.

EC #	Page	Date	Part Affected	Description
EC-SIT3-1	15,16,18	10/10/28	RV1, RV3, RV9,RV10,RV11,C503,C504	Add ESDprotect component for ESD request.
EC-SIT3-2	4	10/10/28	R739,R740,R741,R742,T116,T179	Delete unnecessary component R739,R740,R741,R742. Add T116 ,T179.
EC-SIT3-3	3	10/10/28	R718	change to short pad
	4		R743,R745,R750,R788,R789,R791,R790,R793,R792,R795,R794,R730,R725,R731	
	5		R785,R786	
	6		R124	
	7		R158	
	8		R809,R810,R811,R812	
	9		R825,R827,R831	
	11		R890,R891,R893,R894	
	13		R342,R348,R347,R351,R352	
	14		R119,R117,R112,R110,R108,R105,R103,R101	
	15		R177,R197,R208,R299	
	16		R477,R306,R323	
	18		R132,R133,R141,R142	
	19		R470,R464,R450,R472	
	20		R273,R252	
	21		R176,R253	
	23		R291,R293,R295	
	26		R508,R509,R510,R511	
	29		PR31,PR32,PR37	
	30		PR155,PR218,PR153,PR126,PR207,PR219,PR145,PR222	
	31		PR132,PR206,PR228,PR230,PR238,PR214,PR235,PR9157,PR9160,PR9168,PR9190,PR9183,PR9180,PR711,PR103,PR256,PR243	
	35		PR160,PR287,PR245,PR283,PR241	
EC-SIT3-4	5	10/10/28	R787,R796,R784	delete power jump
	17		R38,R72	
	20		R200	
	31		PJP12,PJP13,PJP6	
	32		PJP14,PJP15	
	33		PJP16,PJP17	
	34		PJP2,PJP18	
EC-SIT3-5	35	10/10/28	PR251,PR249	Change for PSI function
EC-SIT3-6	32,33	10/10/28	PR9162,PR9173	Change for switch phase voltage

EC #	Page	Date	Part Affected	Description

EC #	Page	Date	Part Affected	Description